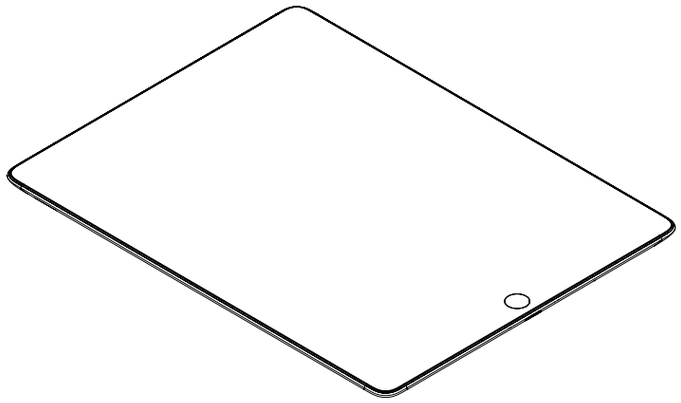
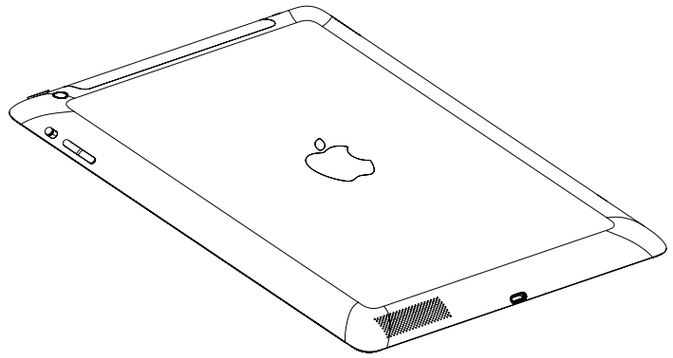
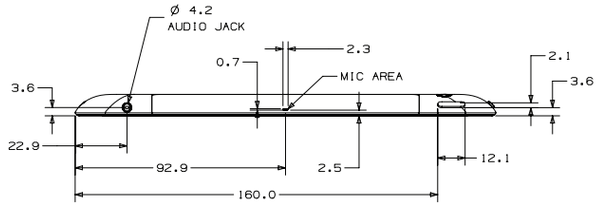
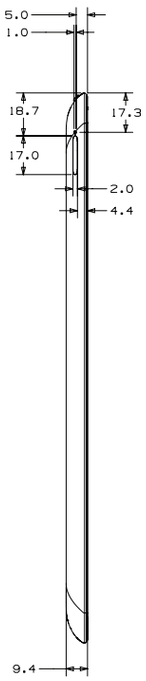
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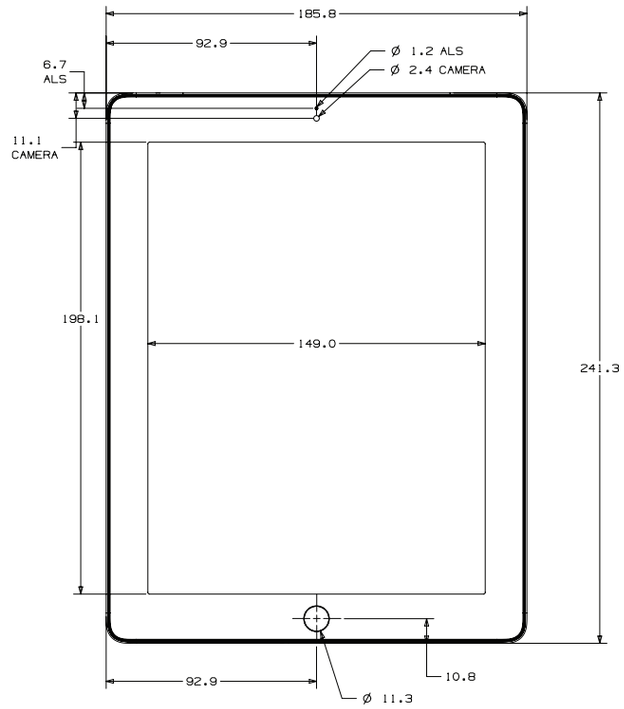
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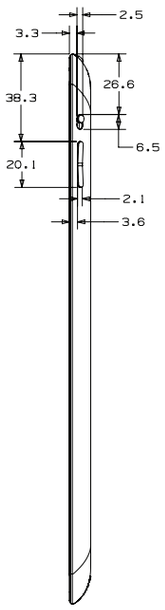


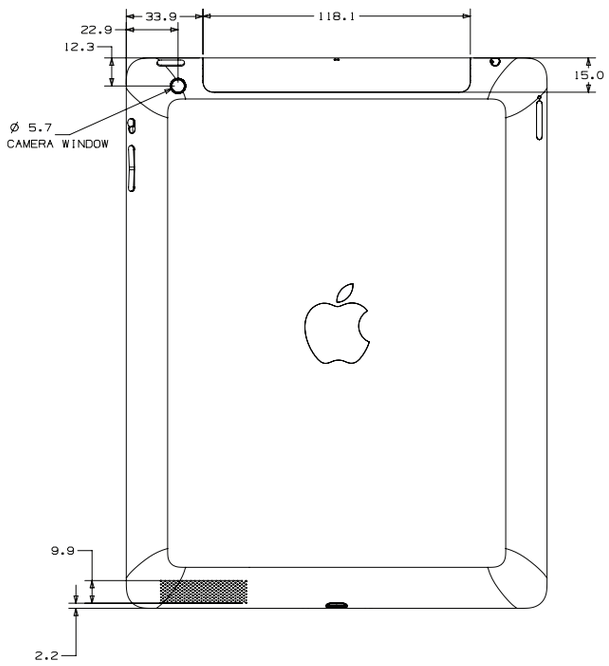


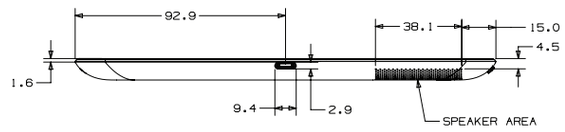


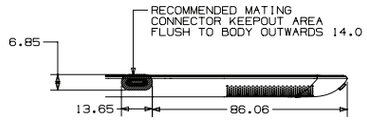


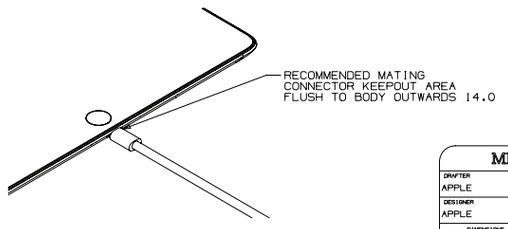












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DIMENSIONS ARE IN MILLIMETERS TOLERANCES X.X ±0.2 X.XX ±0.10 X.XXX ±0.050 ANGLES ±0.5° DO NOT SCALE DRAWINGS		TITLE: IPAD WI-FI + CELLULAR (4TH GENERATION)
		DRAWING NUMBER: REV. 02
THIRD ANGLE PROJECTION	SIZE: B	SCALE: NONE SHT 1 OF 1

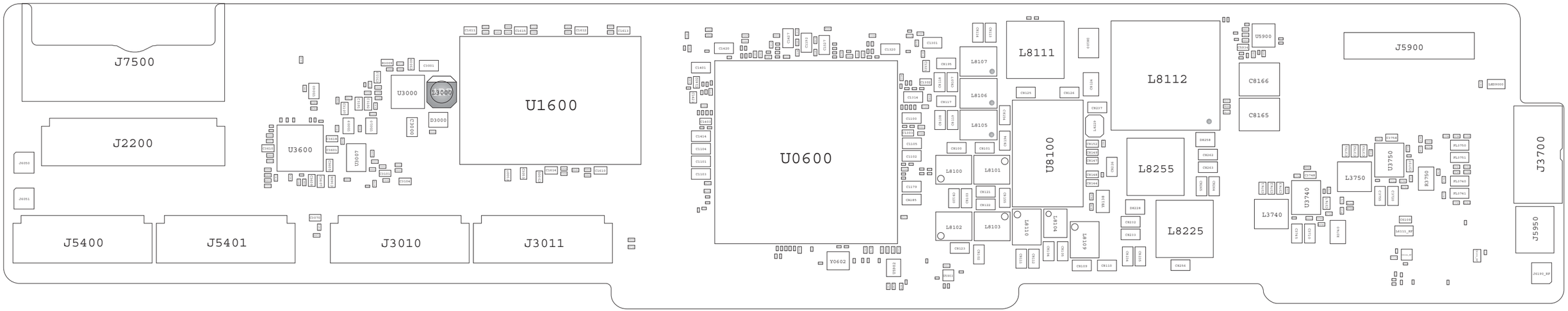
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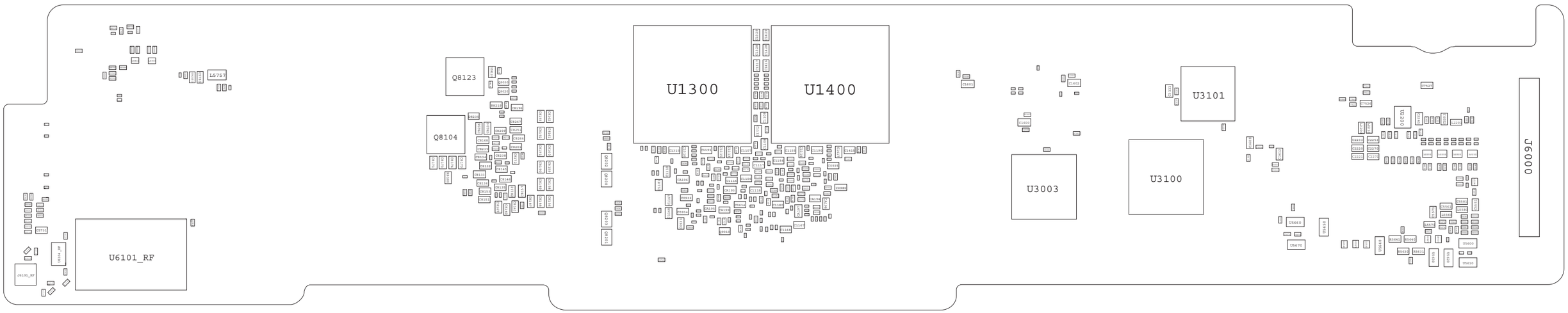
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820-3249-TOP MLB



820-3249-BOT MLB



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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0001554595	PRODUCTION RELEASED	2012-07-26

iPad 4th Gen

LAST_MODIFIED=Thu Jul 26 10:29:36 2012

PDF	CSA	CONTENTS	SYNC MASTER	DATE	(SYSTEM DRI)
1	1	Table of Contents	N/A	N/A	(AMANDA)
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A	(AMANDA)
3	4	BOM TABLES	N/A	N/A	(AMANDA)
4	6	AP: MAIN	N/A	N/A	(TERRY)
5	7	AP: I/Os	N/A	N/A	(AMANDA)
6	8	AP: NAND	N/A	N/A	(TERRY)
7	9	AP: TV,DP,MIPI	N/A	N/A	(TERRY)
8	10	AP: DDR	N/A	N/A	(TERRY)
9	11	AP: POWER	N/A	N/A	(TERRY)
10	12	AP: MISC & ALIASES	N/A	N/A	(TERRY)
11	13	DDR 0 AND 1	N/A	N/A	(TERRY)
12	14	DDR 2 AND 3	N/A	N/A	(TERRY)
13	16	NAND	N/A	N/A	(AMANDA)
14	21	ALIASES	N/A	N/A	(AMANDA)
15	22	VIDEO: EDP CONNECTOR	N/A	N/A	(JOE)
16	30	GRAPE: GROUNDHOG,CONN,BOOST	N/A	N/A	(AMANDA)
17	31	GRAPE: Z1, Z2	N/A	N/A	(AMANDA)
18	36	AUDIO: L81 CODEC	N/A	N/A	(TERRY)
19	37	AUDIO: SPEAKER AMP	N/A	N/A	(TERRY)
20	54	SENSOR FLEX CONN	N/A	N/A	(MARK)
21	55	SENSOR CONN FILTERS 1	N/A	N/A	(MARK)
22	56	SENSOR CONN FILTERS 2	N/A	N/A	(MARK)
23	57	E75 DOCK SUPPORT	N/A	N/A	(JOE)
24	58	IO FLEX CONN	N/A	N/A	(JOE)
25	59	TRISTAR	N/A	N/A	(JOE)
26	60	CONNECTOR: CELLULAR	N/A	N/A	(AMANDA)
27	61	WIFI/BT	N/A	N/A	(MATT)
28	75	POWER: BATTERY CONNECTOR	MADHAVI	12/06/2011	(MADHAVI)
29	81	PMU: ADRIANA PAGE 1	MADHAVI	12/06/2011	(MADHAVI)
30	82	PMU: ADRIANA PAGE 2	MADHAVI	12/06/2011	(MADHAVI)
31	83	PMU: ADRIANA PAGE 3	MADHAVI	12/06/2011	(MADHAVI)
32	90	DEBUG/MISC.	MLB	11/09/2011	(AMANDA)
33	93	TEST/HOLES/FIDUCUALS	N/A	N/A	(AMANDA)
34	121	POWER ALIASES	N/A	N/A	(MADHAVI)
35	150	CONSTRAINTS: MLB RULES	MIKE	11/30/2011	(AMANDA)
36	151	CONSTRAINTS: LOW SPEED BUS	MIKE	11/30/2011	(AMANDA)
37	152	CONSTRAINTS: DISPLAY/AUDIO	MIKE	11/30/2011	(AMANDA)
38	153	CONSTRAINTS: DDR/FMI	MIKE	11/30/2011	(AMANDA)
39	154	CONSTRAINTS: POWER / GND	MIKE	11/30/2011	(AMANDA)

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MLB
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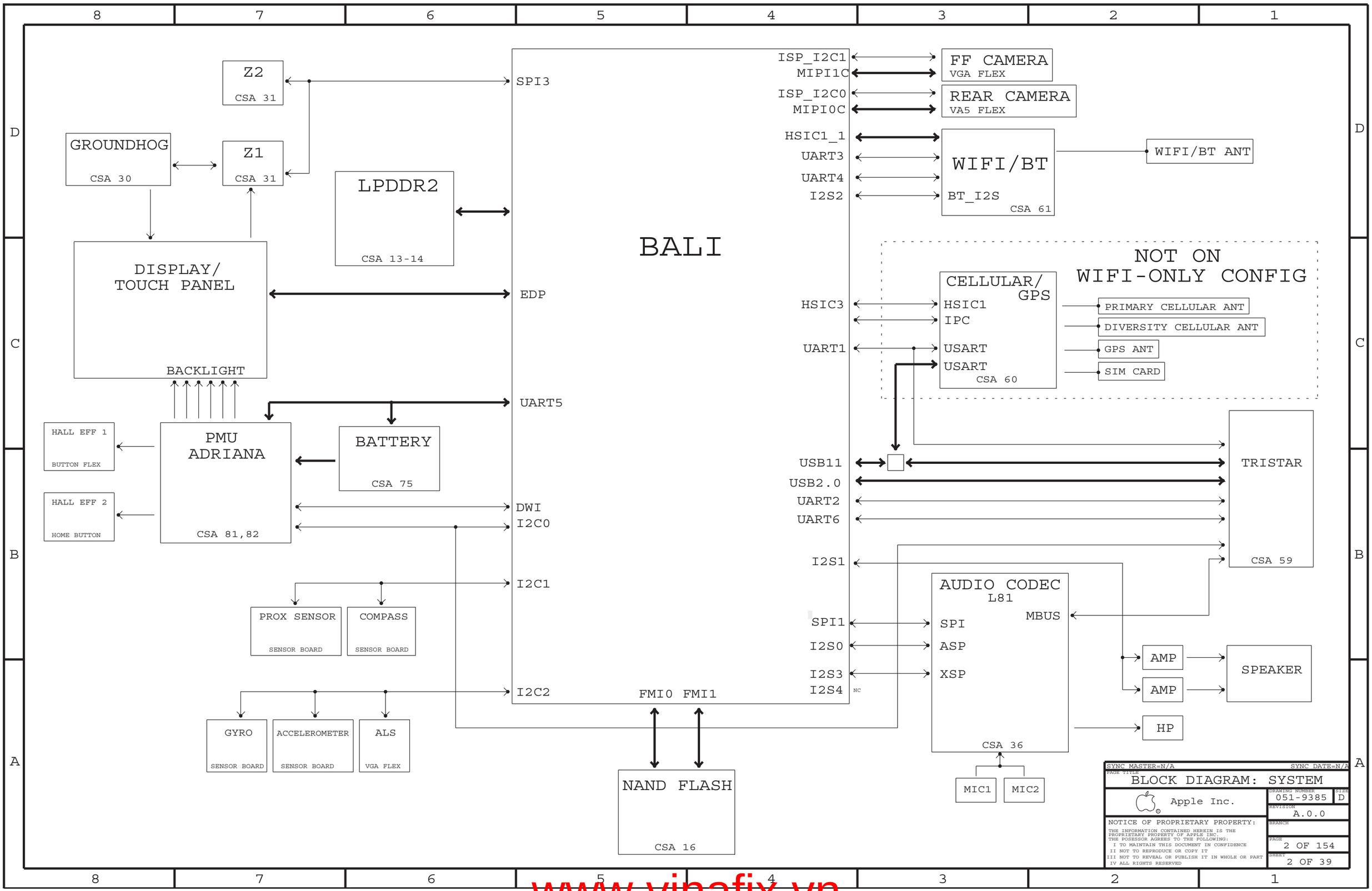
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DRAWING NUMBER: 051-9385 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 154
SHEET: 1 OF 39

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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD: 16GB CONFIG
32GB_PROD: 32GB CONFIG
64GB_PROD: 64 GB CONFIG
DEV: DEV BOARD ONLY

MLB: MLB BOARD ONLY
MLB_A: WIFI ONLY CONFIG
MLB_B: CELLULAR CONFIG
MLB_C: CELLULAR CONFIG
MLB_D: LEGACY CELLULAR CONFIG
MLB_E: LEGACY CELLULAR CONFIG

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

MECHANICAL PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
NAND	806-4195	1	FENCE,NAND,TOP,MLB,X140	PD_FENCE_NAND	CRITICAL	
SOC/PMU	806-3493	1	FENCE,LARGE,TOP,MLB,X140	PD_FENCE_LARGE	CRITICAL	
AUDIO	806-3956	1	FENCE,AMP,MLB,X140	PD_FENCE_AMP	CRITICAL	
GRAPE	806-4196	1	FENCE,1,BTM,MLB,X140	PD_FENCE_BTM1	CRITICAL	
MEMORY	806-3492	1	FENCE,2,BTM,MLB,X140	PD_FENCE_BTM2	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7838	1	EEEE FOR 639-3736 (MLB A 16G)	EEEE_F1WD	CRITICAL	EEEE_MLB_A_16G
825-7838	1	EEEE FOR 639-3737 (MLB A 32G)	EEEE_F1WH	CRITICAL	EEEE_MLB_A_32G
825-7838	1	EEEE FOR 639-3738 (MLB A 64G)	EEEE_F1W8	CRITICAL	EEEE_MLB_A_64G
825-7838	1	EEEE FOR 639-4176 (MLB A 128G)	EEEE_F80Q	CRITICAL	EEEE_MLB_A_128G
825-7838	1	EEEE FOR 639-3263 (MLB B 16G)	EEEE_DWKG	CRITICAL	EEEE_MLB_B_16G
825-7838	1	EEEE FOR 639-3739 (MLB B 32G)	EEEE_F1W7	CRITICAL	EEEE_MLB_B_32G
825-7838	1	EEEE FOR 639-3740 (MLB B 64G)	EEEE_F1WC	CRITICAL	EEEE_MLB_B_64G
825-7838	1	EEEE FOR 639-4177 (MLB B 128G)	EEEE_F80P	CRITICAL	EEEE_MLB_B_128G
825-7838	1	EEEE FOR 639-3741 (MLB C 16G)	EEEE_F1WG	CRITICAL	EEEE_MLB_C_16G
825-7838	1	EEEE FOR 639-3742 (MLB C 32G)	EEEE_F1WF	CRITICAL	EEEE_MLB_C_32G
825-7838	1	EEEE FOR 639-3743 (MLB C 64G)	EEEE_F1W9	CRITICAL	EEEE_MLB_C_64G
825-7838	1	EEEE FOR 639-4178 (MLB C 128G)	EEEE_F80R	CRITICAL	EEEE_MLB_C_128G

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9385	1	SCH,MLB,X140	SCH1	CRITICAL	
820-3249	1	PCBF,MLB,X140	PCB1	CRITICAL	

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0598	1	IC,SOC,H5G,FCBGA1089,0.5MM	U0600	CRITICAL	

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0622	1	IC,PMU,ADRIANA,D2018A1,FCBGA	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0636	2	LPDDR2,533MHZ,512MB,SAMSUNG,35NM	U1300,U1400	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0637	333S0636		U1300,U1400	LPDDR2,533MHZ,HYNIX,38NM
333S0638	333S0636		U1400,U1400	LPDDR2,533MHZ,ELPIDA,38NM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0878	1	TOSHIBA PPN1.5 16GB	U1600	CRITICAL	16GB_PROD

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0879	1	TOSHIBA PPN1.5 32GB	U1600	CRITICAL	32GB_PROD

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0880	1	TOSHIBA PPN1.5 64GB	U1600	CRITICAL	64GB_PROD

128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0912	1	TOSHIBA PPN1.5 128GB	U1600	CRITICAL	128GB_PROD

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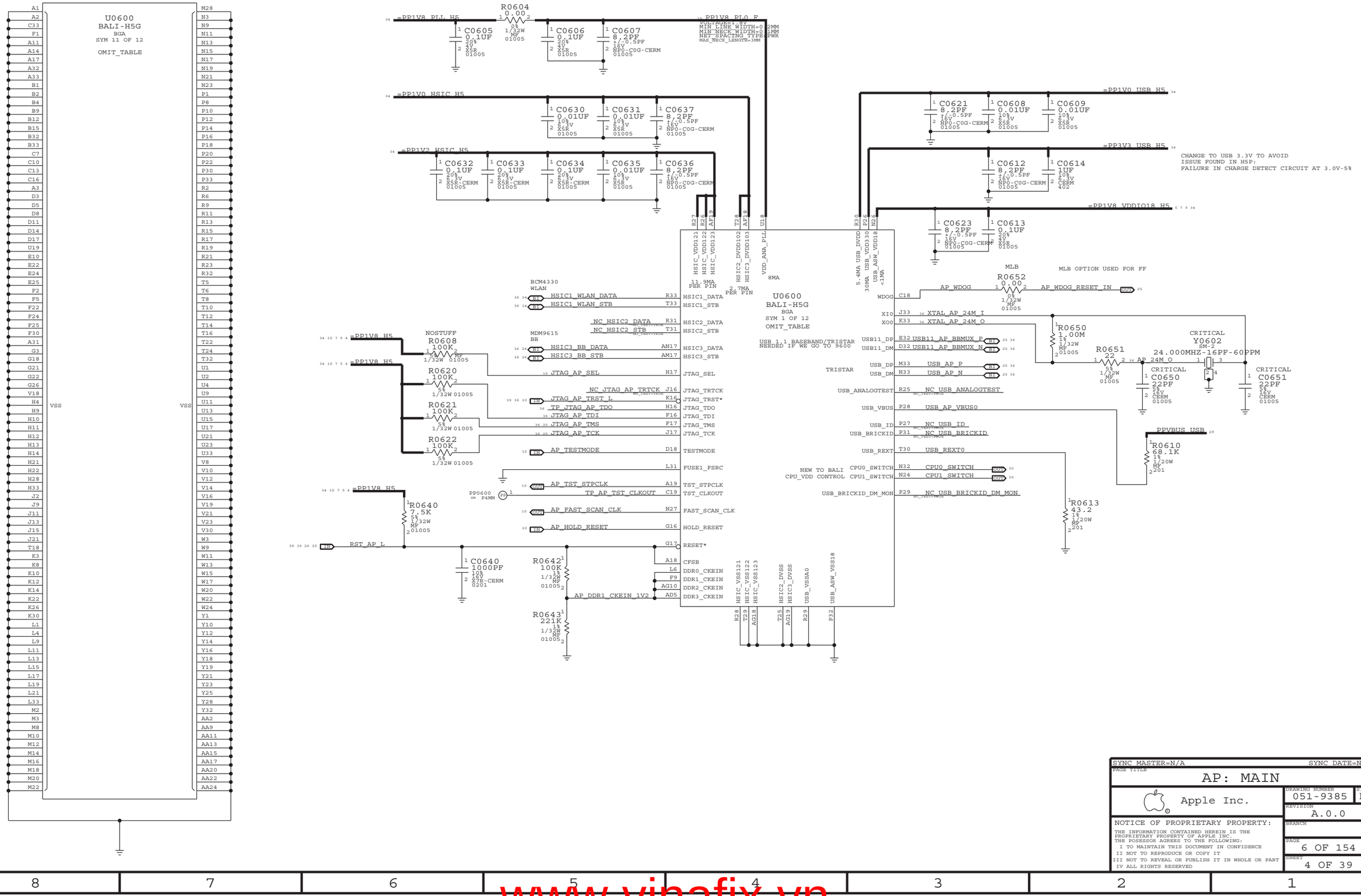
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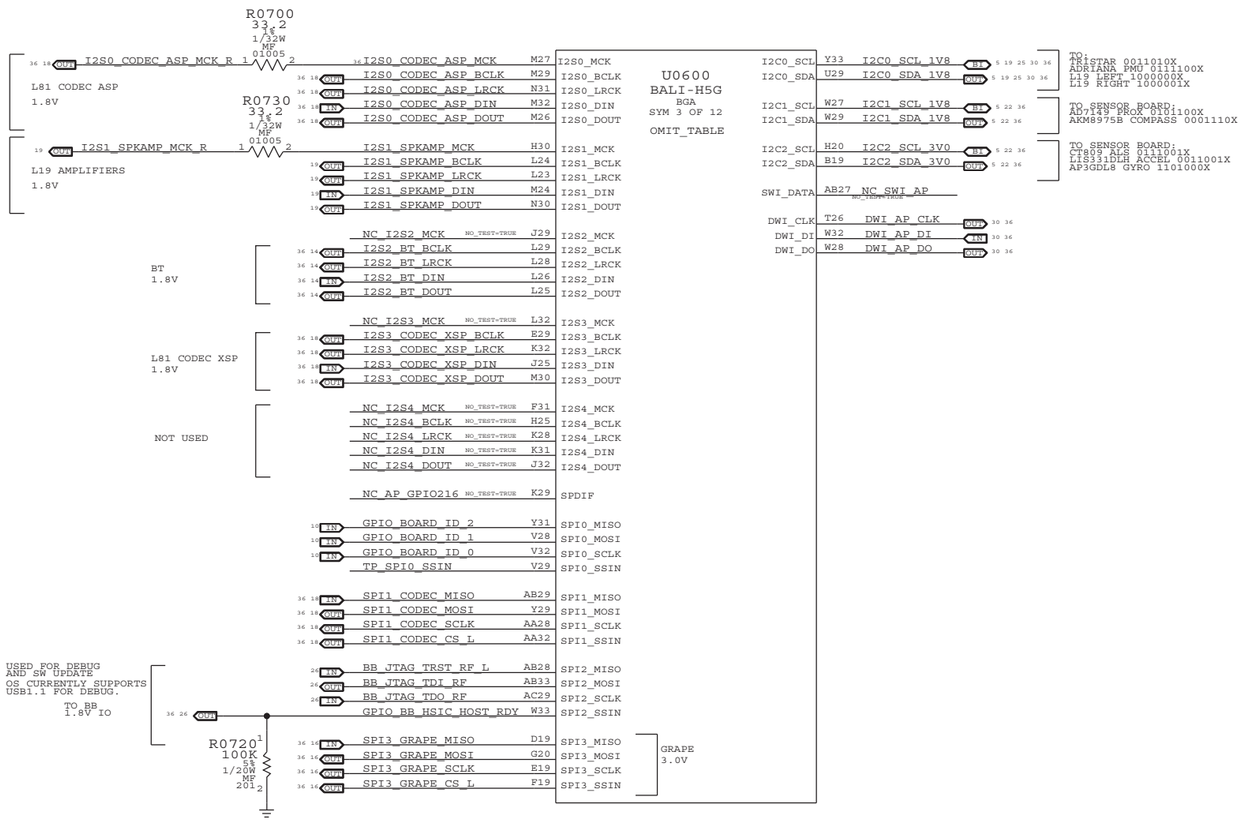
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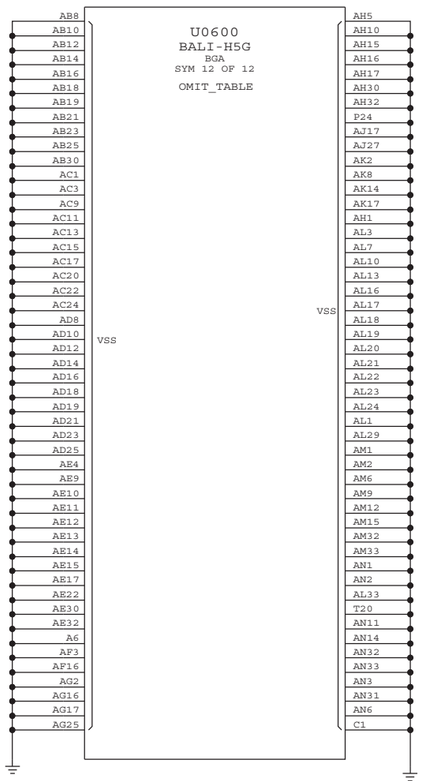
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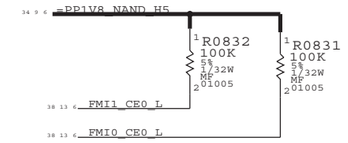
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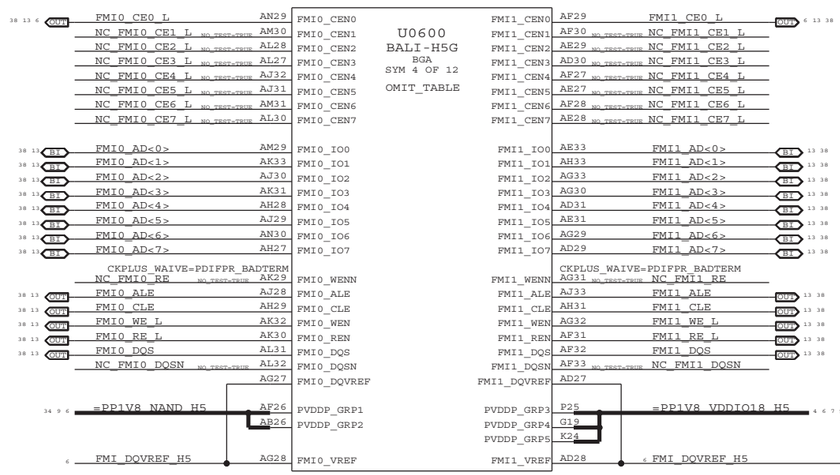
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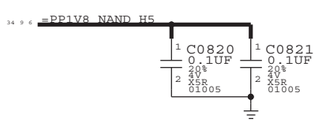
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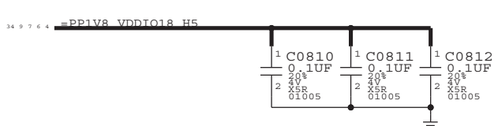
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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=PP1V0_DP_PAD_DVDD_H5 34
C0910 8.2PF ±0.1PF% 25V CERM 0201
=PP1V8_EDP_H5 34
R0911 0 5% 1/20W MF 201
=PP1V8_EDP_AVDD_AUX 33
C0931 56PF 5% 6.3V NPO-C0G 01005
C0928 8.2PF ±0.5PF 16V NPO-C0G-CERM 01005
C0929 8.2PF ±0.5PF 16V NPO-C0G-CERM 01005
C0930 56PF 5% 6.3V NPO-C0G 01005
C0932 0.22UF 20% 6.3V X5R 402
C0933 0.22UF 20% 6.3V X5R 402
C0934 0.22UF 20% 6.3V X5R 402
=PP1V0_EDP_PAD_DVDD_H5 34
C0909 0.1UF 10% 6.3V X5R 201
=PP1V8_DP_H5 34
C0927 0.1UF 20% 4V X5R 01005
C0924 56PF 5% 6.3V NPO-C0G 01005
=PP1V8_VDDIO18_H5 4 6 7 9 34
C0953 0.01UF 10% 6.3V X5R 01005
=PP1V8_VDDIO18_H5 4 6 7 9 34
C0951 0.1UF 20% 4V X5R 01005
C0952 0.01UF 10% 6.3V X5R 01005

NOSTUFF FL0911 240-OHM-0.2A-0.8-OHM
=PP1V8_VDDIO18_H5 34 9 7 6 4 — 0201 — DAC_AP_COMP_FTR
NOSTUFF C0956 0.1UF 10% 6.3V X5R 201
NOSTUFF C0955 0.1UF 10% 6.3V X5R 201
NOSTUFF R0950 6.34K 1% 1/20W MF 201
DAC_AP_VREF 33
DAC_AP_IREF
DAC_AP_COMP

VOLTAGE=1.8V MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM

U0600 BALI-H5G BGA SYM 6 OF 12 OMIT_TABLE

C31	15MA	EDP_PAD_DVDD	DAC_VREF J23
B31	22MA	EDP_PAD_AVDDX	DAC_IREF J24
D29	10MA	EDP_PAD_AVDDP0	DAC_COMP K23
D25		EDP_PAD_AVDD3	EDP_HPD E18
D26		EDP_PAD_AVDD2	EDP_PAD_AUXP C30
C27		EDP_PAD_AVDD1	EDP_PAD_AUXN C29
C28	65MA PER PIN	EDP_PAD_AVDD0	EDP_PAD_TX0P A30
D30	16MA	EDP_PAD_AVDD_AUX	EDP_PAD_TX0N A29
C24	15MA	DP_PAD_DVDD	EDP_PAD_TX1P D28
C23	22MA	DP_PAD_AVDDX	EDP_PAD_TX1N D27
D21	10MA	DP_PAD_AVDDP0	EDP_PAD_TX2P B28
A20		DP_PAD_AVDD3	EDP_PAD_TX2N B27
B20		DP_PAD_AVDD2	EDP_PAD_TX3P C26
E20		DP_PAD_AVDD1	EDP_PAD_TX3N C25
E21	65MA PER PIN	DP_PAD_AVDD0	EDP_PAD_R_BIAS E28
D22	16MA	DP_PAD_AVDD_AUX	EDP_PAD_DC_TP F28
H23	15MA	DAC_AVDD18D	
H24	15MA	DAC_AVDD18A	

NOTE: 0.6V ANALOG REF
NOSTUFF C0957 0.01UF 10% 6.3V X5R 01005
R0921 4.99K 1% 1/32W MF 01005
TP_EDP_AP_ANALOG_TEST

B25	EDP_PAD_AVSS3	
B26	EDP_PAD_AVSS2	
A27	EDP_PAD_AVSS1	
A28	EDP_PAD_AVSS0	
D31	EDP_PAD_DVSS	
C32	EDP_PAD_AVSSX	
B29	EDP_PAD_AVSSP0	
B30	EDP_PAD_AVSS_AUX	
A24	DP_PAD_DVSS	
A23	DP_PAD_AVSSX	
B21	DP_PAD_AVSSP0	
C20	DP_PAD_AVSS3	
F20	DP_PAD_AVSS1	
D20	DP_PAD_AVSS2	
F21	DP_PAD_AVSS0	
B22	DP_PAD_AVSS_AUX	
G23	DAC_AVSS18D	
G24	DAC_AVSS18A	

D33	DAC_OUT3	NC_DAC_AP_OUT3
E33	DAC_OUT2	NC_DAC_AP_OUT2
F33	DAC_OUT1	NC_DAC_AP_OUT1
B18	DP_HPD	NC_DP_HPD
A26	DP_PAD_AUXP	NC_DP_AUX_P
A25	DP_PAD_AUXN	NC_DP_AUX_N
D24	DP_PAD_TX0P	NC_DP_DATA_P<0>
D23	DP_PAD_TX0N	NC_DP_DATA_N<0>
B24	DP_PAD_TX1P	NC_DP_DATA_P<1>
B23	DP_PAD_TX1N	NC_DP_DATA_N<1>
C22	DP_PAD_TX2P	NC_DP_DATA_P<2>
C21	DP_PAD_TX2N	NC_DP_DATA_N<2>
A22	DP_PAD_TX3P	NC_DP_DATA_P<3>
A21	DP_PAD_TX3N	NC_DP_DATA_N<3>
E23	DP_PAD_R_BIAS	DP_R_BIAS
F23	DP_PAD_DC_TP	TP_DP_AP_ANALOG_TEST

NOTE: 0.6V ANALOG REF
R0920 4.99K 1% 1/32W MF 01005
NOSTUFF C0950 0.01UF 10% 6.3V X5R 01005

FL0910 80-OHM-0.2A-0.4-OHM
=PP1V0_MIPI_PLL_H5 34 — 0201-1 — PP1V0_MIPI_PLL_F 33
C0980 1UF 10% 6.3V CERM 402
C0981 0.01UF 10% 6.3V X5R 01005
C0982 56PF 5% 6.3V NPO-C0G 01005

VOLTAGE=1.0V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM

=PP1V0_MIPI_H5 34
C0935 1UF 10% 6.3V CERM 402
C0908 0.1UF 10% 6.3V X5R 201
C0903 0.1UF 10% 6.3V X5R 201
C0904 8.2PF ±0.5PF 16V NP0-C0G-CERM 01005

=PP1V8_MIPI_H5 34
C0907 0.1UF 10% 6.3V X5R 201
PP0V4_MIPI1D
C0960 2.2NF 10% 10V X5R-CERM 0201
C0961 2.2NF 10% 10V X5R-CERM 0201

VOLTAGE=0.4V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM

AF20 AF21 AF22 AF23 AF24 — 40MA MIPI_VDD10 — AH21 AH22 AH23 AH24 AH20 AH23
3.2MA MIPI1D_VDD10_PLL 2MA MIPI1D_VDD18 2MA PER PIN MIPI1D_VREG_0P4V
MIPI_VSS — AG20 AG21 AG22 AG23 AG24

U0600 BALI-H5G BGA SYM 5 OF 12 OMIT_TABLE

NC_MIPI_VSYNC_H5	NO_TEST=TRUE	U27	MIPI_VSYNC
MIPI0C_CAM_RF_DATA_P<0>		AM22	MIPI0C_DPDATA0
MIPI0C_CAM_RF_DATA_N<0>		AN22	MIPI0C_DNDATA0
MIPI0C_CAM_RF_DATA_P<1>		AM21	MIPI0C_DPDATA1
MIPI0C_CAM_RF_DATA_N<1>		AN21	MIPI0C_DNDATA1
NC_MIPI0C_CAM_RF_DATA_P<2>	NO_TEST=TRUE	AM19	MIPI0C_DPDATA2
NC_MIPI0C_CAM_RF_DATA_N<2>	NO_TEST=TRUE	AN19	MIPI0C_DNDATA2
NC_MIPI0C_CAM_RF_DATA_P<3>	NO_TEST=TRUE	AM18	MIPI0C_DPDATA3
NC_MIPI0C_CAM_RF_DATA_N<3>	NO_TEST=TRUE	AN18	MIPI0C_DNDATA3
MIPI0C_CAM_RF_CLK_P		AM20	MIPI0C_DPCLK
MIPI0C_CAM_RF_CLK_N		AN20	MIPI0C_DNCLK

ISP0_FLASH	M25	
ISP0_PRE_FLASH	M31	NC_ISP0_CAM_RF_FLASH
ISP0_SCL	AA27	ISP0_CAM_RF_I2C_SCL
ISP0_SDA	U28	ISP0_CAM_RF_I2C_SDA
ISP1_FLASH	N25	SOCHOT1_L
ISP1_PRE_FLASH	L30	SOCHOT0_L
ISP1_SCL	AA33	ISP1_CAM_FF_I2C_SCL
ISP1_SDA	U30	ISP1_CAM_FF_I2C_SDA
SENSOR0_CLK	V31	ISP0_CAM_RF_CLK_R
SENSOR0_RST	U32	ISP0_CAM_RF_SHUTDOWN
SENSOR1_CLK	U31	ISP1_CAM_FF_CLK_R
SENSOR1_RST	T27	ISP1_CAM_FF_SHUTDOWN_L
MIPI1C_DPDATA0	AM23	MIPI1C_CAM_FF_DATA_P<0>
MIPI1C_DNDATA0	AN23	MIPI1C_CAM_FF_DATA_N<0>
MIPI1C_DPDATA1	AM25	NC_MIPI1C_CAM_FF_DATA_P<1>
MIPI1C_DNDATA1	AN25	NC_MIPI1C_CAM_FF_DATA_N<1>
MIPI1C_DPCLK	AM24	MIPI1C_CAM_FF_CLK_P
MIPI1C_DNCLK	AN24	MIPI1C_CAM_FF_CLK_N

REAR FACING CAM
FRONT FACING CAM

=PP1V8_H5 4 5 7 10 34
R0930 1.00K 5% 1/32W MF 01005
R0931 1.00K 5% 1/32W MF 01005
R0932 1.00K 5% 1/32W MF 01005
R0933 1.00K 5% 1/32W MF 01005

R0900 0.00 5% 1/32W MF 01005
R0940 0.00 5% 1/32W MF 01005

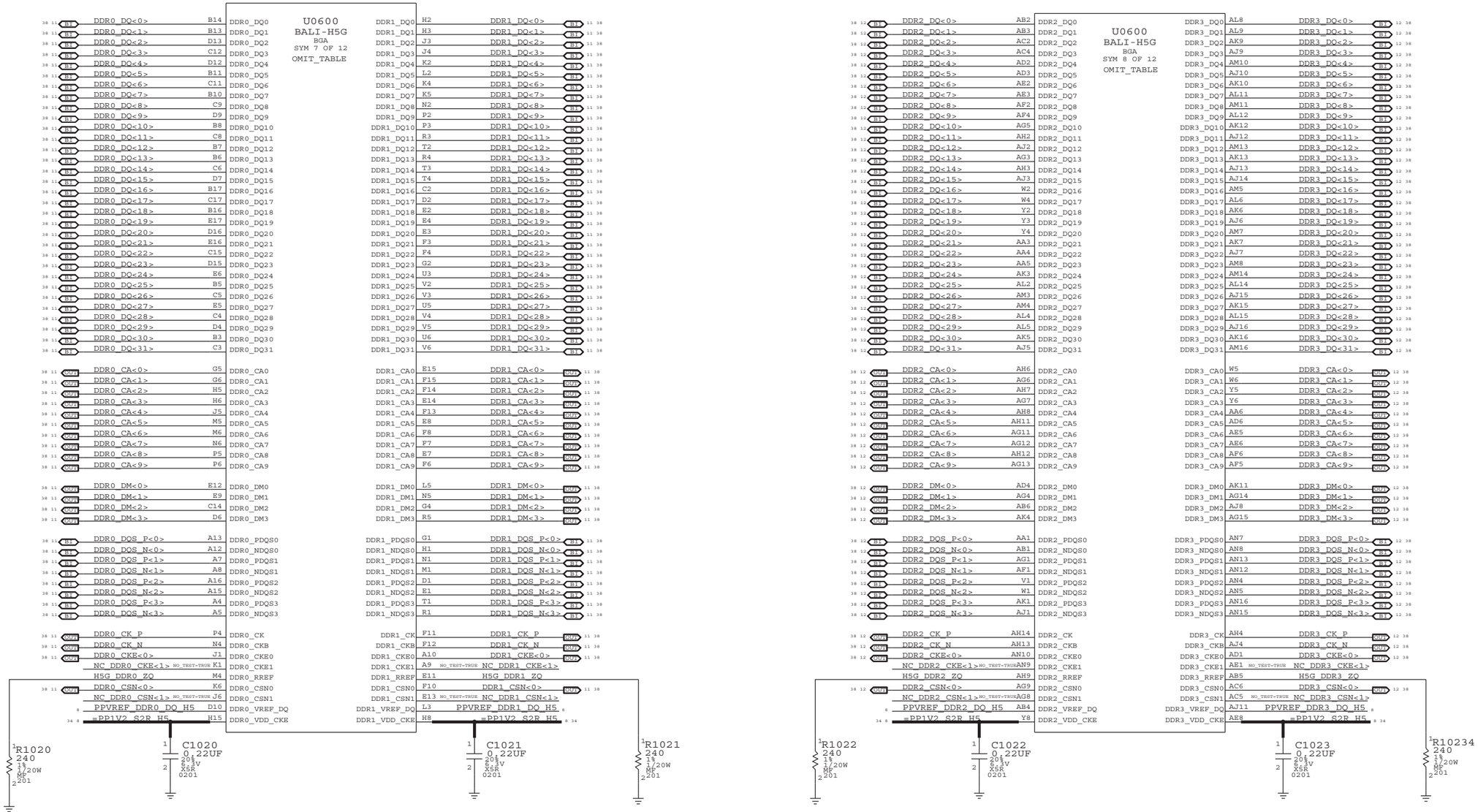
SHUTDOWN IS ACTIVE HIGH
SHUTDOWN IS ACTIVE LOW

=PP1V8_H5 4 5 7 10 34
NOSTUFF R0942 100K 5% 1/32W MF 01005
R0941 100K 5% 1/32W MF 01005
SOCHOT1_L PULL-UP ON CSA 90
SOCHOT1_L 32 7
SOCHOT0_L 7

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE: AP: TV,DP,MIPI
Apple Inc.
DRAWING NUMBER 051-9385 SIZE D
REVISION A.0.0
BRANCH
PAGE 9 OF 154
SHEET 7 OF 39

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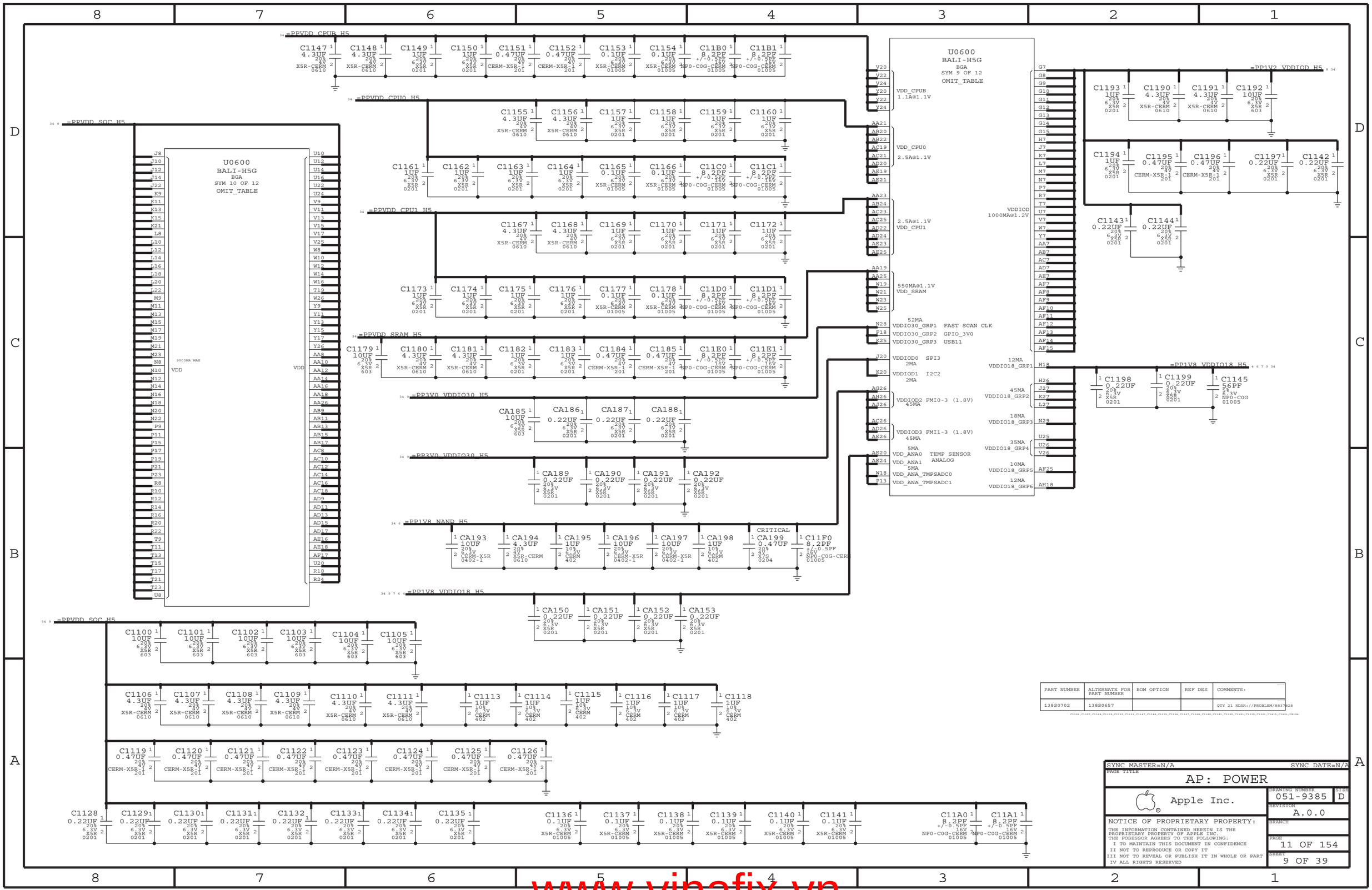
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657			QTY 21 RDAR://PROBLEM/8837828

C1104,C1107,C1108,C1109,C1110,C1111,C1147,C1148,C1155,C1156,C1157,C1158,C1160,C1161,C1190,C1191,C1115,C1121,C1415,C1421,C1434

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: AP: POWER

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DRAWING NUMBER: 051-9385 SIZE: D

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BOOT CONFIG ID

=PP1V8_H5

STUFF FOR FORM FACTOR BOARD

R1200	10K 5% 1/32W MF 01005	STUFF FOR FORM FACTOR BOARD
R1201	10K 5% 1/32W MF 01005	STUFF FOR FORM FACTOR BOARD
R1202	10K 5% 1/32W MF 01005	NOSTUFF
R1203	10K 5% 1/32W MF 01005	NOSTUFF

BOOT_CONFIG[3]	OUT	GPIO_BOOT_CONFIG_3
BOOT_CONFIG[2]	OUT	GPIO_BOOT_CONFIG_2
BOOT_CONFIG[1]	OUT	GPIO_BOOT_CONFIG_1
BOOT_CONFIG[0]	OUT	GPIO_BOOT_CONFIG_0

BOOT_CONFIG[3-0]

CURRENT SETTING ---> 1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

FOR REFERENCE

BOOT_CONFIG[3:0]

0000	SPI0
0001	SPI1
0010	SPI0 W/TEST
0011	SPI1 W/TEST
0100	FMI0 2CS
0101	FMI0 4CS
0110	FMI0 4CS W/TEST
0111	RESERVED
1000	FMI1 2 CS
1001	FMI1 4 CS
1010	FMI1 4CS W/TEST
1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS W/TEST
1111	RESERVED

BOARD ID

=PP1V8_H5

R1220	10K 5% 1/32W MF 01005	MLB_D&MLB_E
R1204	10K 5% 1/32W MF 01005	MLB_C&MLB_E
R1205	10K 5% 1/32W MF 01005	MLB_B&MLB_D
R1206	10K 5% 1/32W MF 01005	DEV

BOARD_ID[3]	OUT	GPIO_BOARD_ID_3
BOARD_ID[2]	OUT	GPIO_BOARD_ID_2
BOARD_ID[1]	OUT	GPIO_BOARD_ID_1
BOARD_ID[0]	OUT	GPIO_BOARD_ID_0

BOARD_ID[3-0]

0000	X140 AP WLAN (MLB A)
0001	X140 DEV WLAN
0010	X140 AP BB_41 (MLB B)
0011	X140 DEV BB_41
0100	X140 AP BB_42 (MLB C)
0101	X140 DEV BB_42
1010	X140 AP BB_26A (MLB D)
1011	X140 DEV BB_26A
1110	X140 AP BB_26 (MLB E)
1111	X140 DEV BB_26

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION

GPIO_BRD_REV2	OUT	
GPIO_BRD_REV1	OUT	
GPIO_BRD_REV0	OUT	

R1207	NOSTUFF 10K 5% 1/32W MF 01005
R1208	NOSTUFF 10K 5% 1/32W MF 01005
R1209	10K 5% 1/32W MF 01005

BRD_REV[2-0]

000	PROTO
001	PROTO 2
010	EVT
CURRENT SETTING ---> 011	DVT

S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

JTAG

R1210	100 5% 1/32W MF 01005	JTAG_AP_SEL
R1211	100 5% 1/32W MF 01005	JTAG_AP_TRST_L

R1260	100K 5% 1/32W MF 01005	AP_TESTMODE
XW1200	NOSTUFF SHORT-01005	AP_TST_STPCLK
XW1201	NOSTUFF SHORT-01005	AP_FAST_SCAN_CLK
XW1202	NOSTUFF SHORT-01005	AP_HOLD_RESET

USB_BRICKID	IN	MAKE_BASE=TRUE	PMU_USB_BRICKID OUT

SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE: AP: MISC & ALIASES

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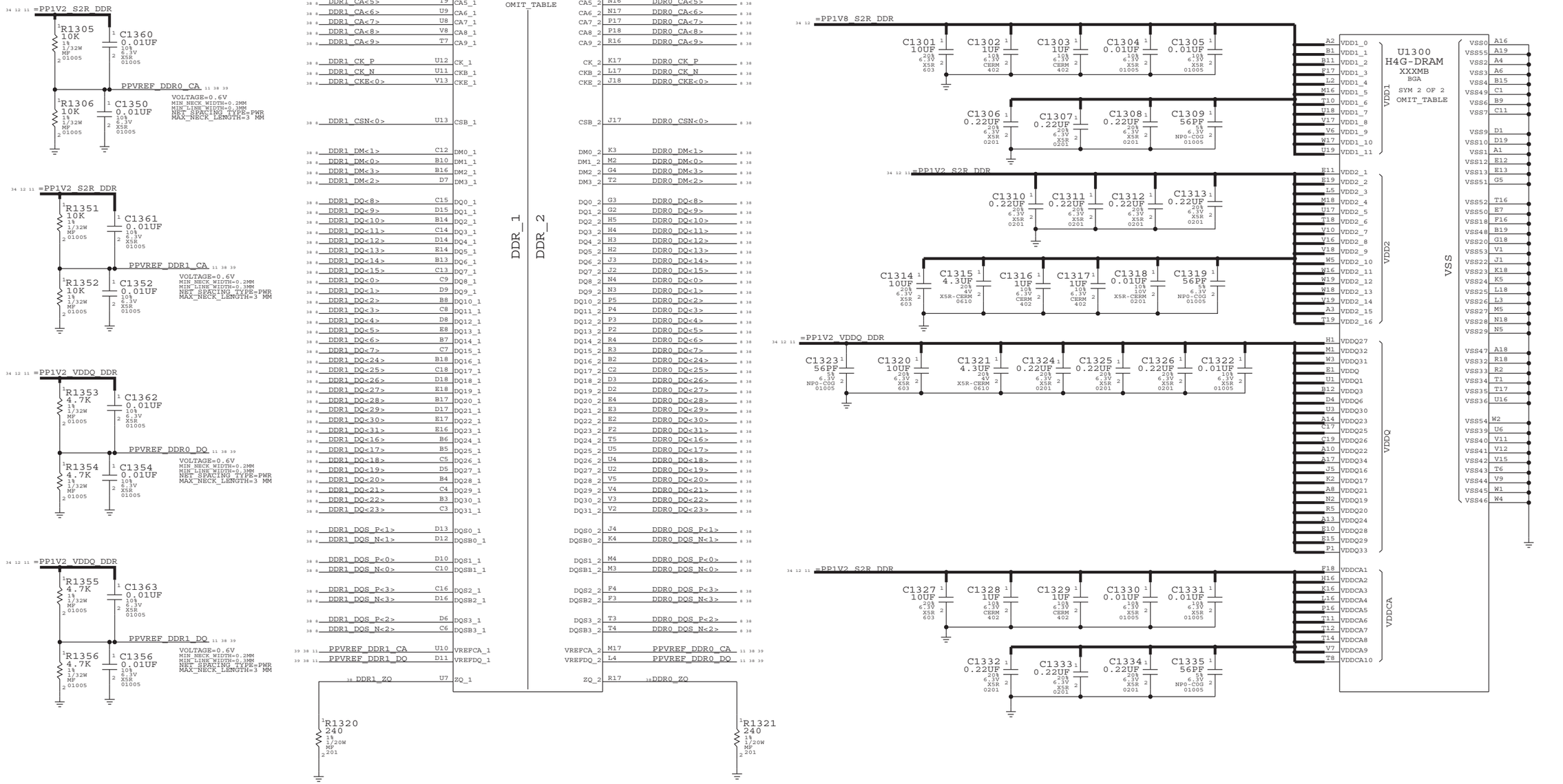
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PAGE TITLE: DDR 0 AND 1

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DRAWING NUMBER: 051-9385 SIZE: D

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PAGE: 13 OF 154

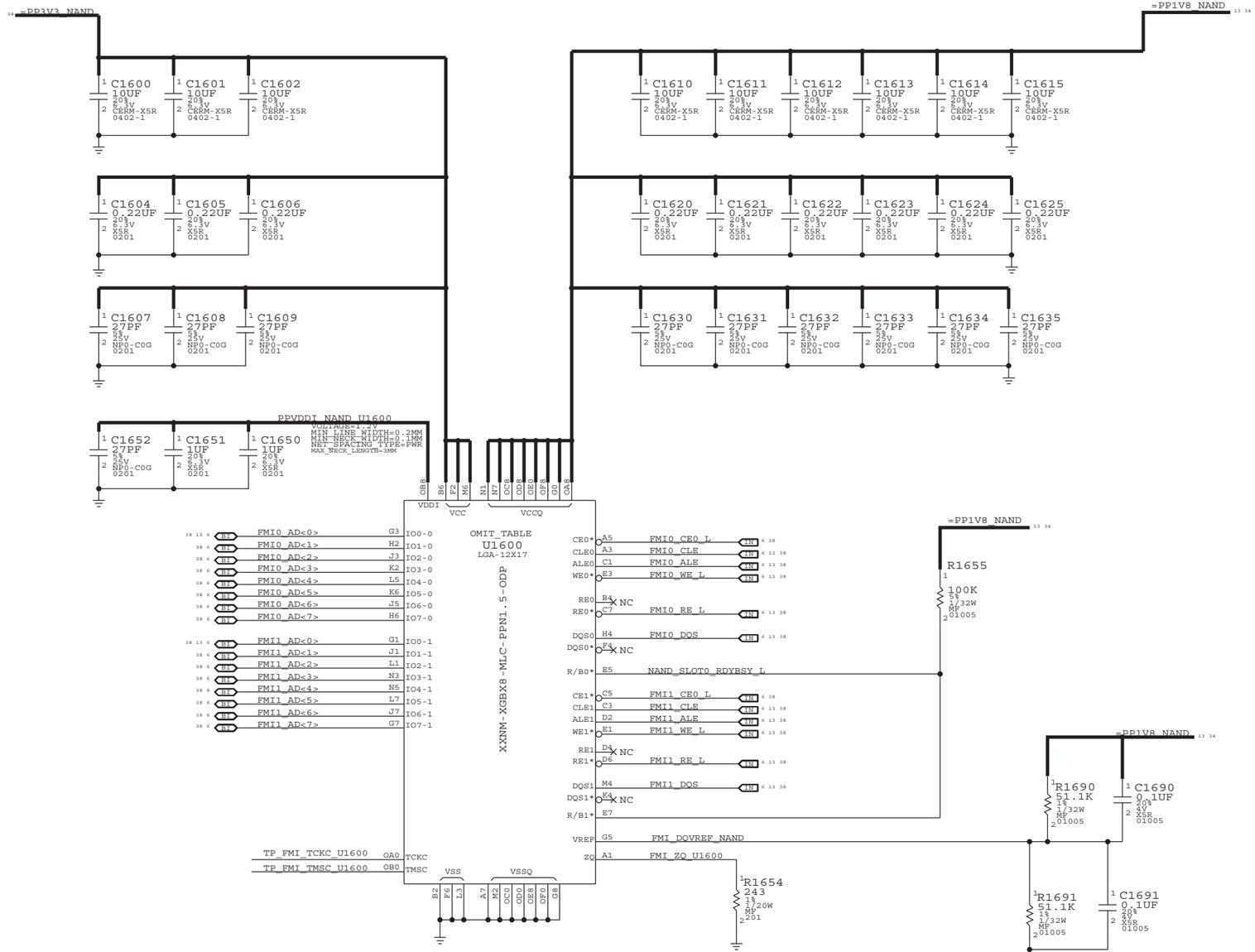
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PAGE TITLE

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WIFI ALIASES

36 4	HSIC1_WLAN_DATA	MAKE_BASE=TRUE	50_HSIC_WLAN_DATA	27
36 4	HSIC1_WLAN_STB	MAKE_BASE=TRUE	50_HSIC_WLAN_STROBE	27
36 5	GPIO_WLAN_HSIC_HOST_RDY	MAKE_BASE=TRUE	AP_HSIC3_RDY	27
36 5	GPIO_WLAN_HSIC_DEV_RDY	MAKE_BASE=TRUE	DEV_HSIC3_RDY	27
30	PMU_GPIO_WLAN_REG_ON	MAKE_BASE=TRUE	WLAN_REG_ON	27
30	PMU_GPIO_WLAN_HOST_WAKE	MAKE_BASE=TRUE	HOST_WAKE_WLAN	27
30	PMU_GPIO_BT_REG_ON	MAKE_BASE=TRUE	BT_REG_ON	27
30	PMU_GPIO_BT_HOST_WAKE	MAKE_BASE=TRUE	HOST_WAKE_BT	27
5	GPIO_BT_WAKE	MAKE_BASE=TRUE	BT_WAKE	27
36 5	UART3_BT_RXD	MAKE_BASE=TRUE	BT_UART_TXD	27
36 5	UART3_BT_TXD	MAKE_BASE=TRUE	BT_UART_RXD	27
36 5	UART3_BT_CTS_L	MAKE_BASE=TRUE	BT_UART_RTS_L	27
36 5	UART3_BT_RTS_L	MAKE_BASE=TRUE	BT_UART_CTS_L	27
36 30	PMU_GPIO_CLK_32K_WLAN	MAKE_BASE=TRUE	CLK32K_AP	27
36 5	I2S2_BT_BCLK	MAKE_BASE=TRUE	BT_PCM_CLK	27
36 5	I2S2_BT_DOUT	MAKE_BASE=TRUE	BT_PCM_IN	27
36 5	I2S2_BT_DIN	MAKE_BASE=TRUE	BT_PCM_OUT	27
36 5	I2S2_BT_LRCK	MAKE_BASE=TRUE	BT_PCM_SYNC	27
36 5	UART4_WLAN_RXD	MAKE_BASE=TRUE	WLAN_UART_TXD	27
36 5	UART4_WLAN_TXD	MAKE_BASE=TRUE	WLAN_UART_RXD	27
5	GPIO_WL_HSIC_RESUME	MAKE_BASE=TRUE	WLAN_HSIC3_RESUME	27
34	VDDIO_WLAN_BT_1V8	MAKE_BASE=TRUE	PP_WL_BT_VDDIO_AP	27

SYNC_MASTER=N/A SYNC_DATE=N/A

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ALIASES

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EDP CONNECTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0667	155S0583		L2242,L5500,L5510,L5520,L5530,L5540,L5930,L5931	RDAR://PROBLEM/8616060, RADAR://PROBLEM/9015335
155S0625	155S0559		L2202,L2212,L2222,L2232	RDAR://PROBLEM/9017591

=PP3V3_LCD
PPVCC_MAIN
C2240 0.1UF 10% 6.3V X5R 201
C2239 0.1UF 10% 6.3V X5R 201
U2200 SLG5AP302 TDFN CRITICAL
VDD CAP ON GND D S
LCD_RAMP
IN PM_LCDVDD_PWREN
R2205 100K 1% 1/20W MF 201
C2241 3900PF 10% 50V X7R 0402

LAYOUT NOTE:
PUT THERMAL VIAS AROUND U2200 IN CASE OF SHORTED CONDITION

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
PP3V3_S0_LCD_FERR
CRITICAL L2201 FERR-120-OHM-1.5A 0402A
C2203 0.1UF 10% 6.3V X5R 201
C2202 1UF 10% 6.3V CERM 402
NOSTUFF R2290 47K 5% 1/20W MF 201
C2230 82PF 5% 25V NP0-C0G-CERM 0201
C2232 8.2PF +/-0.1PF% 25V CER 0201
C2206 1000PF 10% 16V X7R-CERM 0201

R2280 1.00M CONN_EDP_DATA_EMI_N<0>
C2280 1.2PF NOSTUFF +/-0.1PF 16V NP0-C0G 01005
R2281 1.00M CONN_EDP_DATA_EMI_P<0>
C2281 1.2PF NOSTUFF +/-0.1PF 16V NP0-C0G 01005
R2282 1.00M CONN_EDP_DATA_EMI_N<1>
C2282 1.2PF NOSTUFF +/-0.1PF 16V NP0-C0G 01005
R2283 1.00M CONN_EDP_DATA_EMI_P<1>
C2283 1.2PF NOSTUFF +/-0.1PF 16V NP0-C0G 01005
R2284 1.00M CONN_EDP_DATA_EMI_N<2>
C2284 1.2PF NOSTUFF +/-0.1PF 16V NP0-C0G 01005
R2285 1.00M CONN_EDP_DATA_EMI_P<2>
C2285 1.2PF NOSTUFF +/-0.1PF 16V NP0-C0G 01005
R2286 1.00M CONN_EDP_DATA_EMI_N<3>
C2286 1.2PF NOSTUFF +/-0.1PF 16V NP0-C0G 01005
R2287 1.00M CONN_EDP_DATA_EMI_P<3>
C2287 1.2PF NOSTUFF +/-0.1PF 16V NP0-C0G 01005

PP3V3_S0_LCD_FERR
R2240 100K 1% 1/32W MF 01005
R2241 100K 1% 1/32W MF 01005

EDP_AUX_N C2250 0.1UF 201 6.3V 10% X5R EDP_AUX_EMI_N
EDP_AUX_P C2251 0.1UF 201 6.3V 10% X5R EDP_AUX_EMI_P
CRITICAL L2242 90-OHM-50MA TCM0605-1 SYM_VER-2
CONN_EDP_AUX_EMI_N
CONN_EDP_AUX_EMI_P

EDP_DATA_N<0> C2242 0.1UF 201 6.3V 10% X5R EDP_DATA_EMI_N<0>
EDP_DATA_P<0> C2243 0.1UF 201 6.3V 10% X5R EDP_DATA_EMI_P<0>
CRITICAL L2212 TCM0806-4SM 12-OHM-100MA-8.5GHZ
CONN_EDP_DATA_EMI_N<0>
CONN_EDP_DATA_EMI_P<0>

EDP_DATA_N<1> C2244 0.1UF 201 6.3V 10% X5R EDP_DATA_EMI_N<1>
EDP_DATA_P<1> C2245 0.1UF 201 6.3V 10% X5R EDP_DATA_EMI_P<1>
CRITICAL L2222 TCM0806-4SM 12-OHM-100MA-8.5GHZ
CONN_EDP_DATA_EMI_N<1>
CONN_EDP_DATA_EMI_P<1>

EDP_DATA_N<2> C2246 0.1UF 201 6.3V 10% X5R EDP_DATA_EMI_N<2>
EDP_DATA_P<2> C2247 0.1UF 201 6.3V 10% X5R EDP_DATA_EMI_P<2>
CRITICAL L2232 TCM0806-4SM 12-OHM-100MA-8.5GHZ
CONN_EDP_DATA_EMI_N<2>
CONN_EDP_DATA_EMI_P<2>

EDP_DATA_N<3> C2248 0.1UF 201 6.3V 10% X5R EDP_DATA_EMI_N<3>
EDP_DATA_P<3> C2249 0.1UF 201 6.3V 10% X5R EDP_DATA_EMI_P<3>
CRITICAL L2202 TCM0806-4SM 12-OHM-100MA-8.5GHZ
CONN_EDP_DATA_EMI_N<3>
CONN_EDP_DATA_EMI_P<3>

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
PP3V3_LCDVDD_SW_F

518S0827
CRITICAL
J2200
502250-8051-B
F-RT-SM

EDP_HPD
R2242 100K 1% 1/32W MF 01005

CONN_EDP_AUX_EMI_P
NC
CONN_EDP_AUX_EMI_N
CONN_EDP_DATA_EMI_N<0>
CONN_EDP_DATA_EMI_P<0>
CONN_EDP_DATA_EMI_N<1>
CONN_EDP_DATA_EMI_P<1>
CONN_EDP_DATA_EMI_N<2>
CONN_EDP_DATA_EMI_P<2>
CONN_EDP_DATA_EMI_N<3>
CONN_EDP_DATA_EMI_P<3>
J2200_29_GND
LED_IO_6_B
LED_IO_5_B
LED_IO_4_B
LED_IO_3_B
LED_IO_2_B
LED_IO_1_B
J2200_36_GND
LED_IO_6_A
LED_IO_5_A
LED_IO_4_A
LED_IO_3_A
LED_IO_2_A
LED_IO_1_A
J2200_43_GND

R2295 0 5% 1/20W MF 201 J2200_29_GND
R2296 0 5% 1/20W MF 201 J2200_36_GND
R2297 0 5% 1/20W MF 201 J2200_43_GND

=PPLED_REG_B
CRITICAL L2210 FERR-240-OHM-25%-300MA 0402
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
PPLED_BACK_REG_B
C2253 100PF 5% 50V CERM 0402
C2270 820PF 10% 50V CERM 0402
C2271 8.2PF +/-0.25PF 50V CERM 402-1

=PPLED_REG_A
CRITICAL L2200 FERR-240-OHM-25%-300MA 0402
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
PPLED_BACK_REG_A
C2233 100PF 5% 50V CERM 0402
C2220 820PF 10% 50V CERM 0402
C2221 8.2PF +/-0.25PF 50V CERM 402-1

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE
VIDEO: EDP CONNECTOR

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DRAWING NUMBER 051-9385 SIZE D
REVISION A.0.0
BRANCH
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

CONNECTORS TO GRAPE FLEX

R3070 0 5% 1/20W MF 201 — AG_SHLD_TST_FLEX — AG_SHLD_TST

NOSTUFF R3071 0 5% 1/20W MF 201

C3070 0.1UF 10% 25V X5R 402

P/N 518S0828

MATES WITH LEFTMOST GRAPE FLEX TAIL

CRITICAL
J3010
502250-8037-B
F-RT-SM

MT_PANEL_OUT<36>	37	36	MT_PANEL_OUT<37>
MT_PANEL_OUT<38>	35	34	MT_PANEL_OUT<39>
	33	32	
MT_PANEL_IN<29>	31	30	MT_PANEL_IN<28>
MT_PANEL_IN<27>	29	28	MT_PANEL_IN<26>
MT_PANEL_IN<25>	27	26	MT_PANEL_IN<24>
MT_PANEL_IN<23>	25	24	MT_PANEL_IN<22>
MT_PANEL_IN<21>	23	22	MT_PANEL_IN<20>
MT_PANEL_IN<19>	21	20	MT_PANEL_IN<18>
MT_PANEL_IN<17>	19	18	MT_PANEL_IN<16>
MT_PANEL_IN<15>	17	16	MT_PANEL_IN<14>
MT_PANEL_IN<13>	15	14	MT_PANEL_IN<12>
MT_PANEL_IN<11>	13	12	MT_PANEL_IN<10>
MT_PANEL_IN<9>	11	10	MT_PANEL_IN<8>
MT_PANEL_IN<7>	9	8	MT_PANEL_IN<6>
MT_PANEL_IN<5>	7	6	MT_PANEL_IN<4>
MT_PANEL_IN<3>	5	4	MT_PANEL_IN<2>
MT_PANEL_IN<1>	3	2	MT_PANEL_IN<0>
AG_SHLD_TST_FLEX	1		

MATES WITH RIGHTMOST GRAPE FLEX TAIL

CRITICAL
J3011
502250-8037-B
F-RT-SM

MT_PANEL_OUT<1>	37	36	MT_PANEL_OUT<0>
MT_PANEL_OUT<3>	35	34	MT_PANEL_OUT<2>
MT_PANEL_OUT<5>	33	32	MT_PANEL_OUT<4>
MT_PANEL_OUT<7>	31	30	MT_PANEL_OUT<6>
MT_PANEL_OUT<9>	29	28	MT_PANEL_OUT<8>
MT_PANEL_OUT<11>	27	26	MT_PANEL_OUT<10>
MT_PANEL_OUT<13>	25	24	MT_PANEL_OUT<12>
MT_PANEL_OUT<15>	23	22	MT_PANEL_OUT<14>
MT_PANEL_OUT<17>	21	20	MT_PANEL_OUT<16>
MT_PANEL_OUT<19>	19	18	MT_PANEL_OUT<18>
MT_PANEL_OUT<21>	17	16	MT_PANEL_OUT<20>
MT_PANEL_OUT<23>	15	14	MT_PANEL_OUT<22>
MT_PANEL_OUT<25>	13	12	MT_PANEL_OUT<24>
MT_PANEL_OUT<27>	11	10	MT_PANEL_OUT<26>
MT_PANEL_OUT<29>	9	8	MT_PANEL_OUT<28>
MT_PANEL_OUT<31>	7	6	MT_PANEL_OUT<30>
MT_PANEL_OUT<33>	5	4	MT_PANEL_OUT<32>
MT_PANEL_OUT<35>	3	2	MT_PANEL_OUT<34>
	1		

PP18V_GRAPE — C3005 0.1UF 10% 25V X5R 402 — C3007 0.1UF 10% 25V X5R 402 — C3053 0.1UF 10% 25V X5R 402 — =PP3V0_GRAPE_MARIO1 — C3006 0.1UF 10% 6.3V X5R 201

VDDH — VCC_DIG

U3003
GROUNDHOG
BGA
CRITICAL
OMIT

MUX_IN<0>	B1	MUX0	
MUX_IN<1>	C1	MUX1	
MUX_IN<2>	E1	MUX2	
MUX_IN<3>	F2	MUX3	
MUX_IN<4>	H1	MUX4	
MUX_IN<5>	J1	MUX5	
MUX_IN<6>	J2	MUX6	
MUX_IN<7>	J3	MUX7	
MUX_IN<8>	K4	MUX8	
MUX_IN<9>	H5	MUX9	
MUX_IN<10>	I5	MUX10	
MUX_IN<11>	J8	MUX11	
MUX_IN<12>	J9	MUX12	
MUX_IN<13>	K8	MUX13	
MUX_IN<14>	J10	MUX14	
MUX_IN<15>	I10	MUX15	
MUX_IN<16>	H10	MUX16	
MUX_IN<17>	F11	MUX17	
MUX_IN<18>	C11	MUX18	
MUX_IN<19>	E10	MUX19	
NC	A11	MUX20	
NC	B4	MUX21	
NC	A5	MUX22	
NC	A2	MUX23	
Z1_BON_L<0>	C7	BON_L0	
Z1_BON_L<1>	A7	BON_L1	
Z1_BON_L<2>	B7	BON_L2	
Z1_BON_L<3>	B8	BON_L3	
Z1_BON_L<4>	A8	BON_L4	
Z1_BON_L<5>	C8	BON_L5	
NC	C6		
NC	D3		
NC	D4		
NC	D5		
NC	D6		
NC	D8		
NC	D9		
NC	E4		
NC	E8		
NC	F4		
NC	F5		
NC	F8		
NC	F9		
NC	G4		
NC	G9		
NC	H3		
NC	H4		
NC	H7		
NC	H8		
NC	H9		
NC	J6		
NC	K7		

NC

VSTM0	A1	MT_PANEL_OUT<0>	
VSTM1	B2	MT_PANEL_OUT<1>	
VSTM2	C2	MT_PANEL_OUT<2>	
VSTM3	D1	MT_PANEL_OUT<3>	
VSTM4	D2	MT_PANEL_OUT<4>	
VSTM5	E2	MT_PANEL_OUT<5>	
VSTM6	F1	MT_PANEL_OUT<6>	
VSTM7	G1	MT_PANEL_OUT<7>	
VSTM8	G2	MT_PANEL_OUT<8>	
VSTM9	I1	MT_PANEL_OUT<9>	
VSTM10	H2	MT_PANEL_OUT<10>	
VSTM11	I2	MT_PANEL_OUT<11>	
VSTM12	K1	MT_PANEL_OUT<12>	
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VSTM14	I3	MT_PANEL_OUT<14>	
VSTM15	K3	MT_PANEL_OUT<15>	
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VSTM19	H6	MT_PANEL_OUT<19>	
VSTM20	K5	MT_PANEL_OUT<20>	
VSTM21	J5	MT_PANEL_OUT<21>	
VSTM22	I7	MT_PANEL_OUT<22>	
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VSTM29	I9	MT_PANEL_OUT<29>	
VSTM30	J11	MT_PANEL_OUT<30>	
VSTM31	I11	MT_PANEL_OUT<31>	
VSTM32	H11	MT_PANEL_OUT<32>	
VSTM33	G11	MT_PANEL_OUT<33>	
VSTM34	G10	MT_PANEL_OUT<34>	
VSTM35	F10	MT_PANEL_OUT<35>	
VSTM36	C10	MT_PANEL_OUT<36>	
VSTM37	D10	MT_PANEL_OUT<37>	
VSTM38	E11	MT_PANEL_OUT<38>	
VSTM39	D11	MT_PANEL_OUT<39>	
VSTM40	B11	NC	
VSTM41	B10	NC	
VSTM42	C4	NC	
VSTM43	A4	NC	
VSTM44	B5	NC	
VSTM46	A3	NC	
VSTM45	C5	NC	
VSTM47	B3	NC	
A_AD_R0	A10	Z1_B_ADR<0>	
A_AD_R1	B9	Z1_B_ADR<1>	
A_AD_R2	A9	Z1_B_ADR<2>	

GND — G8 G7 G6 G5 F7 F6 E7 B6 B5 E3 D7 C9

BOOST CONVERTOR

MIN_NECK_MIDTH SHOULD BE 0.4MM

CRITICAL
L3000
4.7UH-700MA-280MOHM
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.2MM
VLF

VR_BOOST_L — VR_BOOST_SW

CRITICAL
D3000
SOD-323
B0520WSXG

VOLTAGE=18V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM NET_SPACING_TYPE=PWR

PP18V_R_GRAPE — R3066 0.1 1% 1/20W MF 201 — PP18V_GRAPE

LOAD CURRENT ~ 153UA

VOLTAGE=18V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=PWR

=PP3V0_GRAPE — C3009 0.1UF 10% 25V X5R 402

C3008 33PF 5% 25V NPO-COG 0201

R3009 1M 1% 1/16W MF-LF 402

C3000 1UF 10% 25V X5R 603-1

VIN — CRITICAL — U3000 TPS61045 QFN-1 — FB — VR_BOOST_FBK — CTRL — PM_BOOST_EN — SW — DO — NCX — L

THRML PAD — PGND — GND

C3001 2.2UF 10% 6.3V X5R 603

C3002 470PF 10% 16V X5R-X7R-CERM 0201

R3012 71.5K 1% 1/20W MF 201

AGND_U3000 — MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.2MM — XW3000 SM

=PP3V0_GRAPE — R3025 10K 5% 1/20W MF 201

SPI3_GRAPE_SCLK	MAKE_BASE=TRUE	GRAPE_SCLK	
SPI3_GRAPE_CS_L	MAKE_BASE=TRUE	GRAPE_CS_L	
SPI3_GRAPE_MOSI	MAKE_BASE=TRUE	GRAPE_MOSI	
GPIO_GRAPE_RST_L	MAKE_BASE=TRUE	RST_GRAPE_Z1_L	
		RST_GRAPE_Z2_L	
SPI3_GRAPE_MISO	MAKE_BASE=TRUE	GRAPE_MISO	

TO Z2

=PP3V0_GRAPE — R3030 10K 5% 1/20W MF 201 — R3031 10K 5% 1/20W MF 201 — C3030 0.1UF 10% 6.3V X5R 201 — C3031 0.1UF 10% 6.3V X5R 201 — R3032 3.3K 5% 1/20W MF 201 — R3033 10K 5% 1/20W MF 201 — =PP3V0_GRAPE

U3007
PQFP1
CRITICAL
SN74AVCH4T245RSV
VCCA VCCB
(A -> B)
DIR_U3007
GND

SPI3_GRAPE_SCLK	IN	1A1	1B1 — Z1_SCLK — OUT
SPI3_GRAPE_CS_L	IN	2A1	2B1 — Z2_H_CS_L — OUT
SPI3_GRAPE_MOSI	IN	1A2	1B2 — Z1_MISO — OUT
GPIO_GRAPE_FW_DNLD_EN_L	IN	2A2	2B2 — Z1_CS_OE — OUT

TO Z1/Z2

APN:311S0485

=PP1V8_MISC — C3060 0.1UF 10% 6.3V X5R 201 — =PP3V0_GRAPE

U3060
SN74LVC1T45YZPR
BGA
VCCA VCCB
DIR
GND

GPIO_GRAPE_IRQ_L	OUT	A	B — GPIO_GRAPE_IRQ_3V0_L — IN

NOSTUFF R3060 0 5% 1/20W MF 201

=PP3V0_GRAPE — C3050 0.1UF 10% 6.3V X5R 201

U3010
SN74LVC1G126DRYR-M
LLP
CRITICAL
VCC
GND
NC

Z1_CS_OE	IN	OE*	
Z2_H_CS_L	IN	A	Y — Z1_CS_L — OUT

=PP3V0_GRAPE — C3041 0.1UF 10% 6.3V X5R 201

U3009
SN74LVC1G125DRYR-M
LLP
CRITICAL
NC
NC

SPI3_GRAPE_MISO	OUT		Z1_MOSI — IN
Z1_CS_OE	IN	OE*	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

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PAGE TITLE
GRAPE: GROUNDHOG,CONN,BOOST

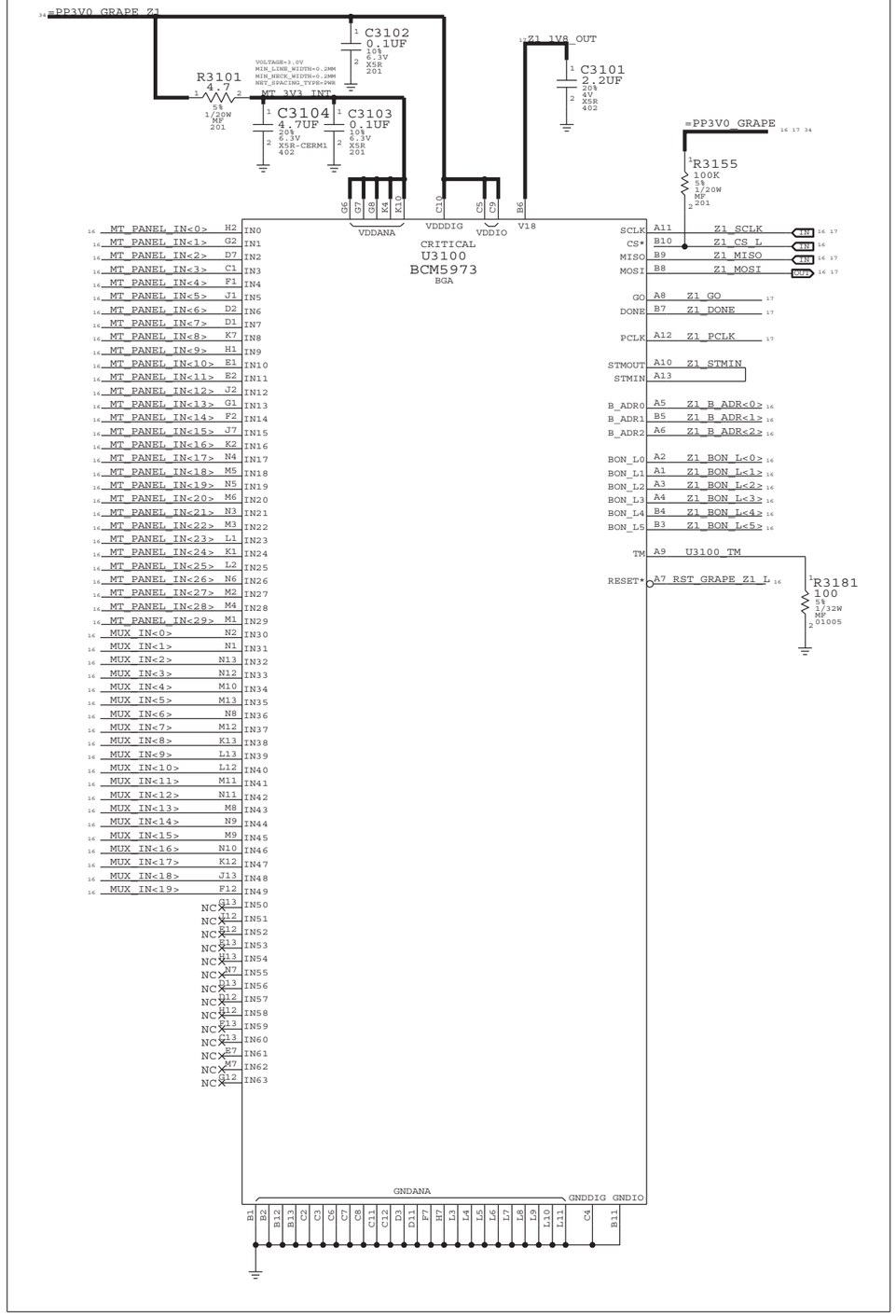
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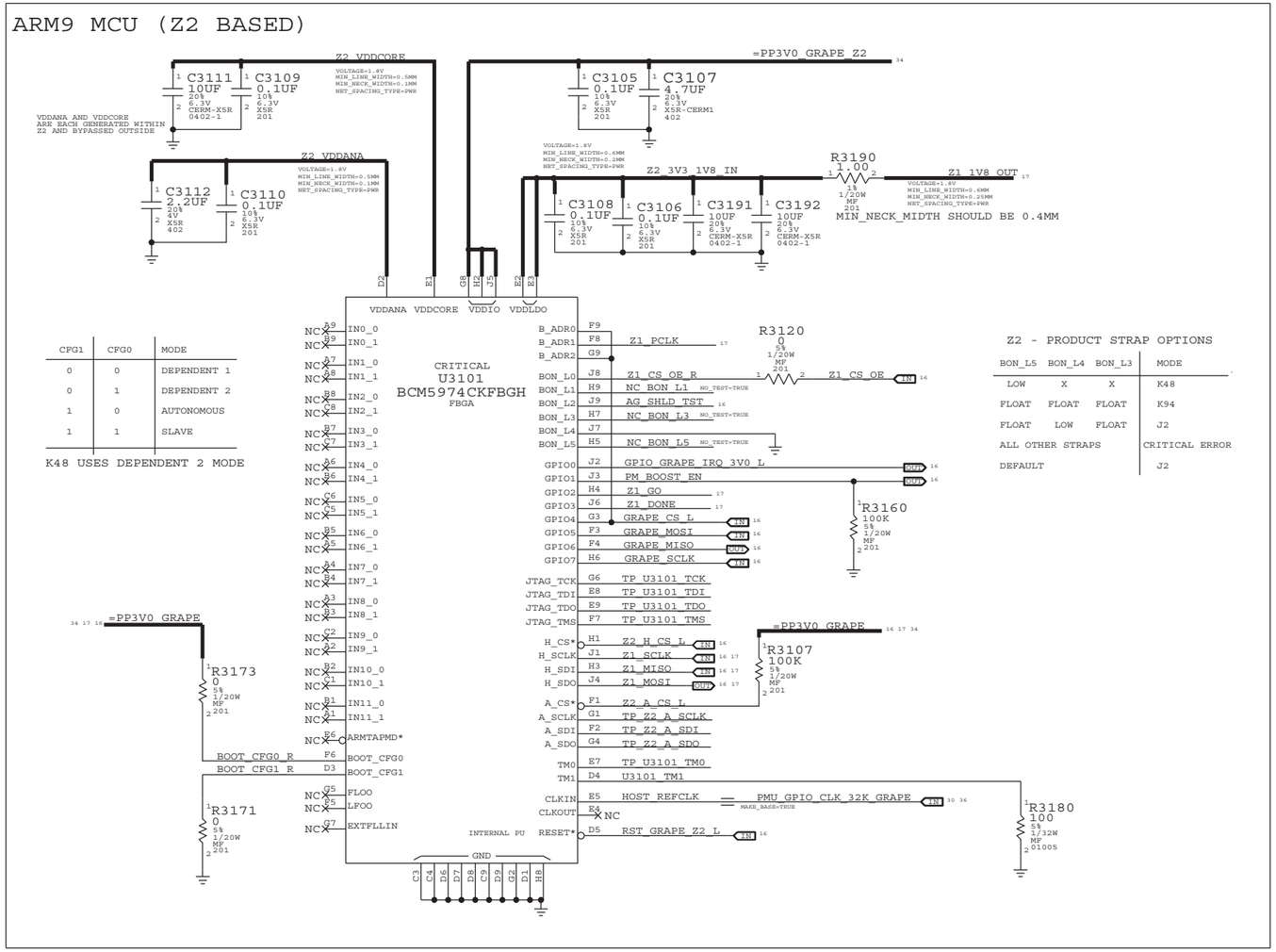
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ZEPHYR 1+ ASIC



ARM9 MCU (Z2 BASED)



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PAGE TITLE: GRAPE: Z1, Z2

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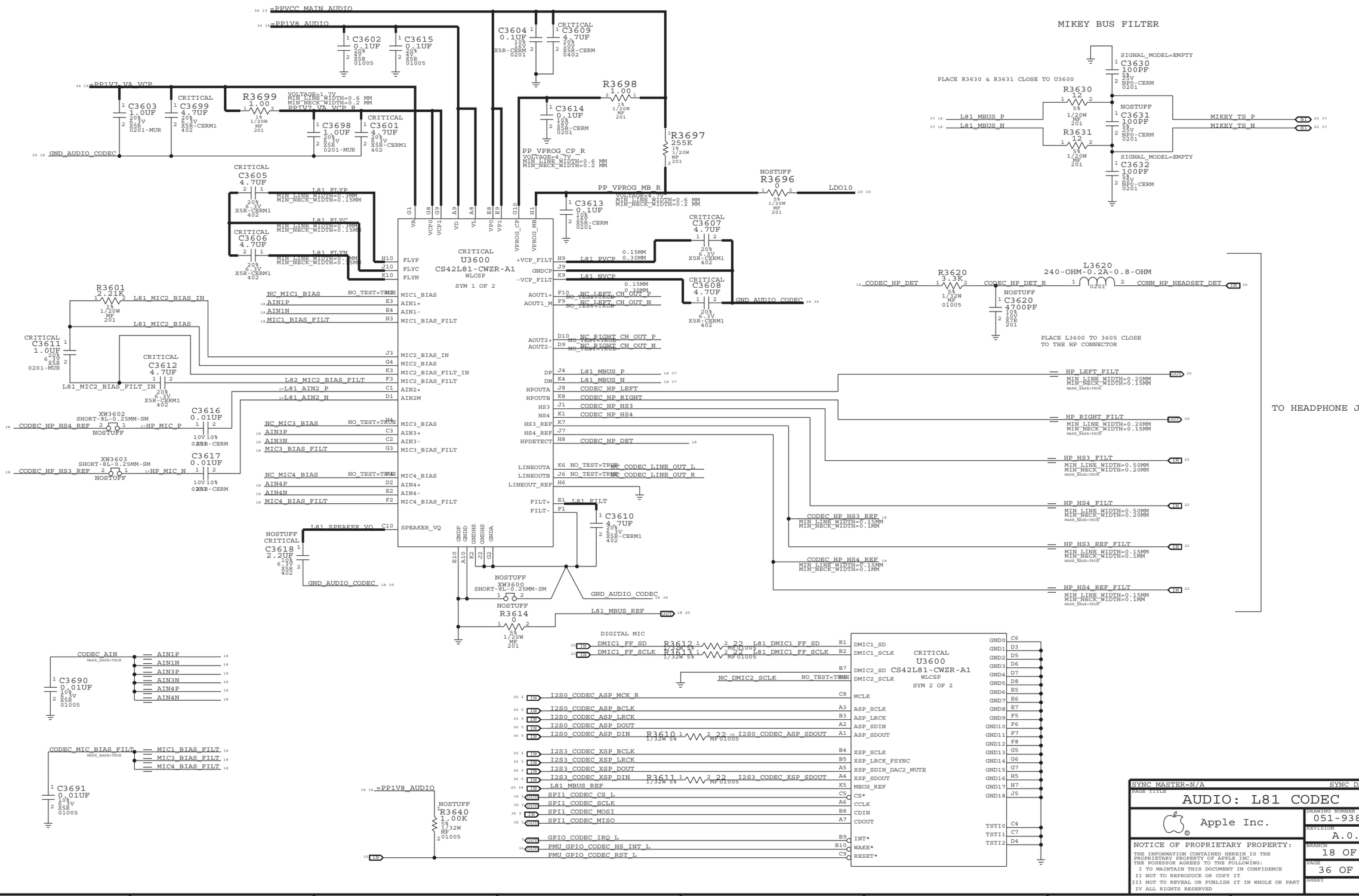
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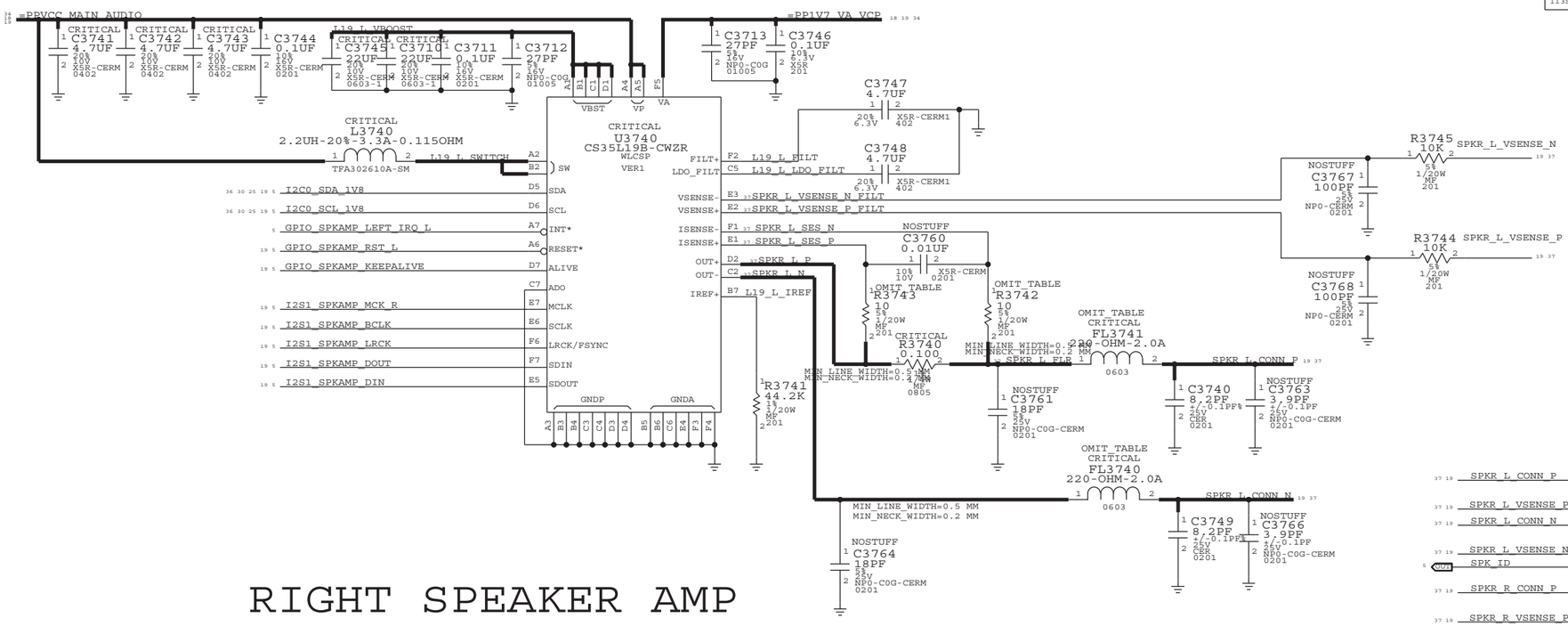
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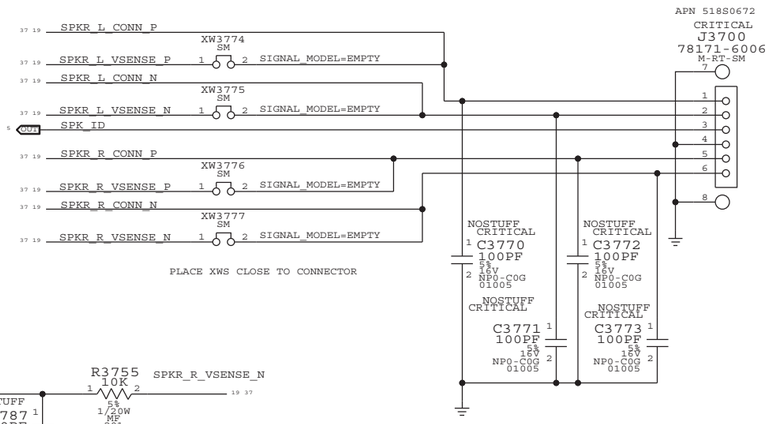
LEFT SPEAKER AMP

I2C ADDRESS: 1000000X

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0002	4	RES,MF,1/20W,0.00HM,5,0201,SMD	R3742,R3743,R3752,R3753	?	?
113S0022	4	RES,MF,1/10W,00HM,5,0603,SMD,LF	FL3740,FL3741,FL3750,FL3751	?	?

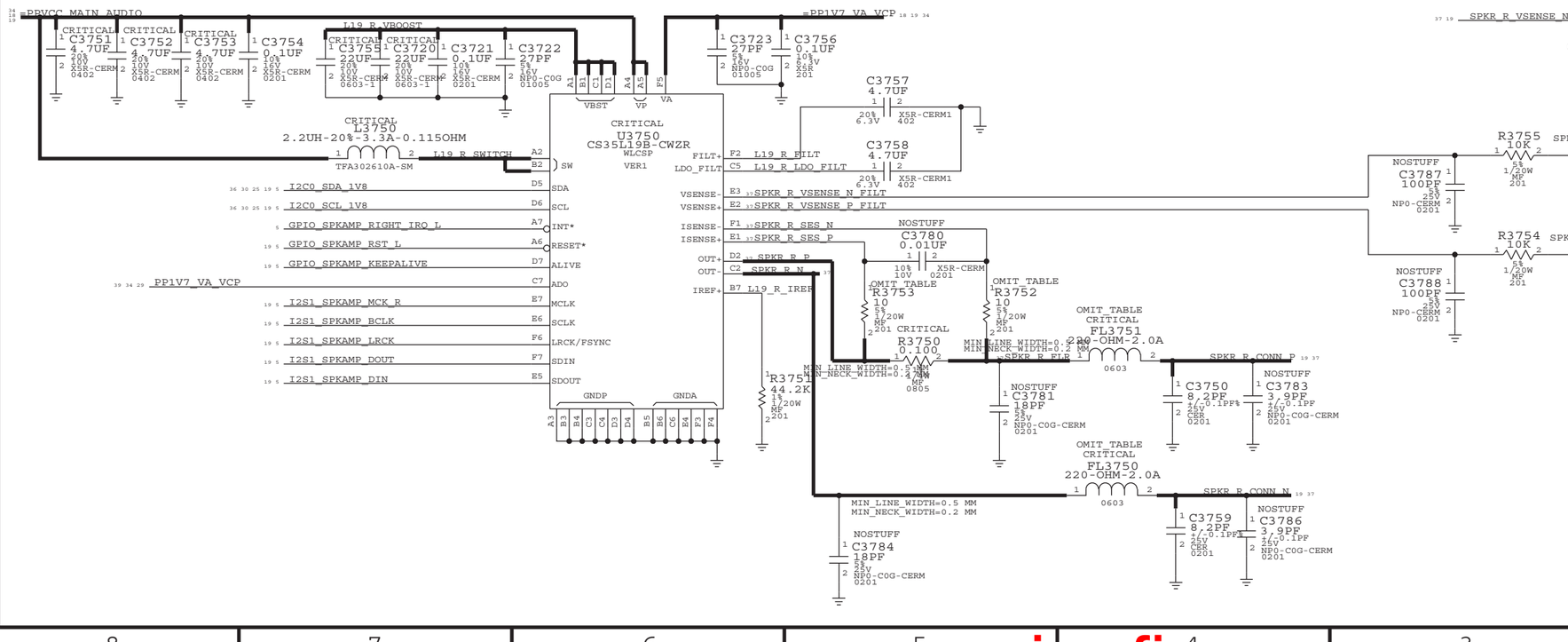


SPEAKER CONNECTOR



RIGHT SPEAKER AMP

I2C ADDRESS: 1000001X

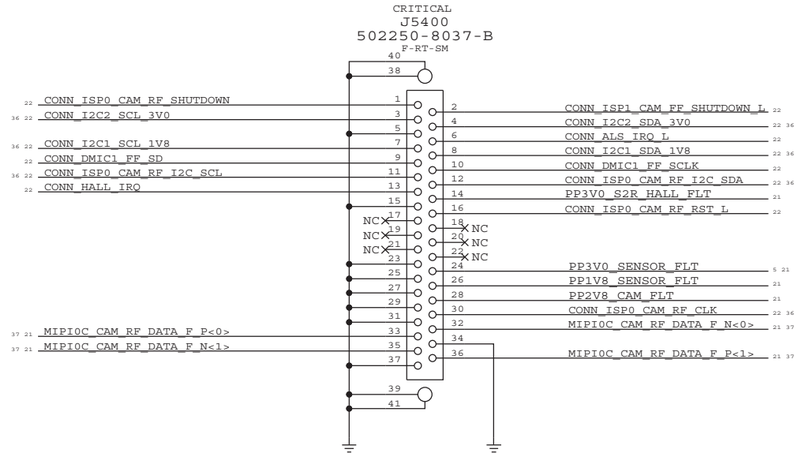


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PAGE TITLE	AUDIO: SPEAKER AMP
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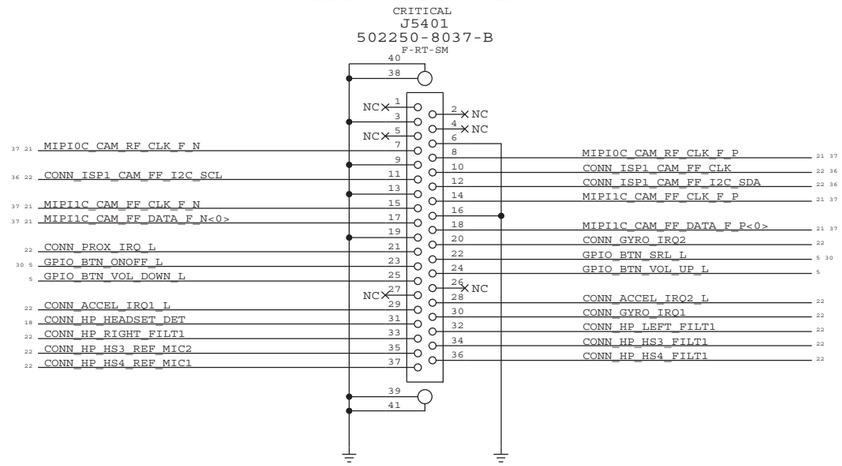
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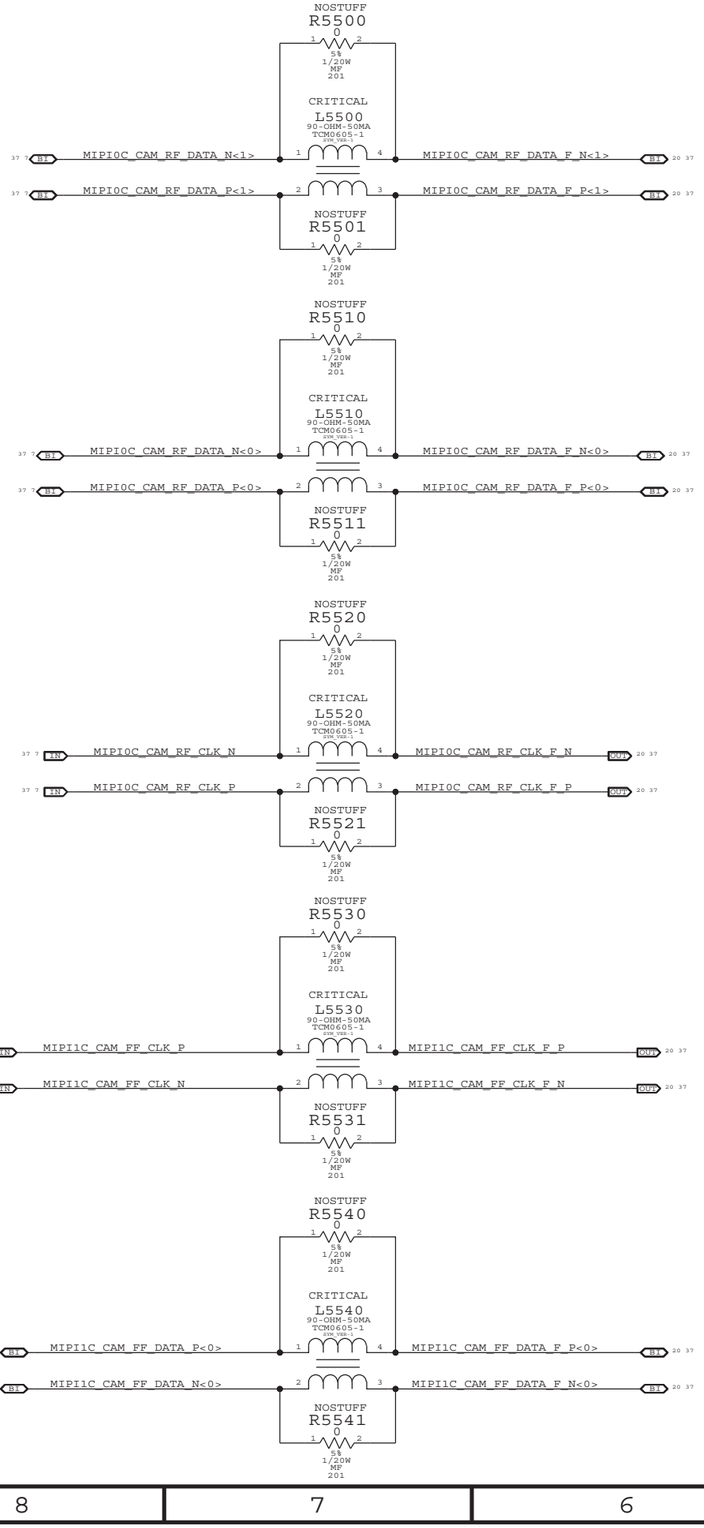
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SENSOR FLEX CONN

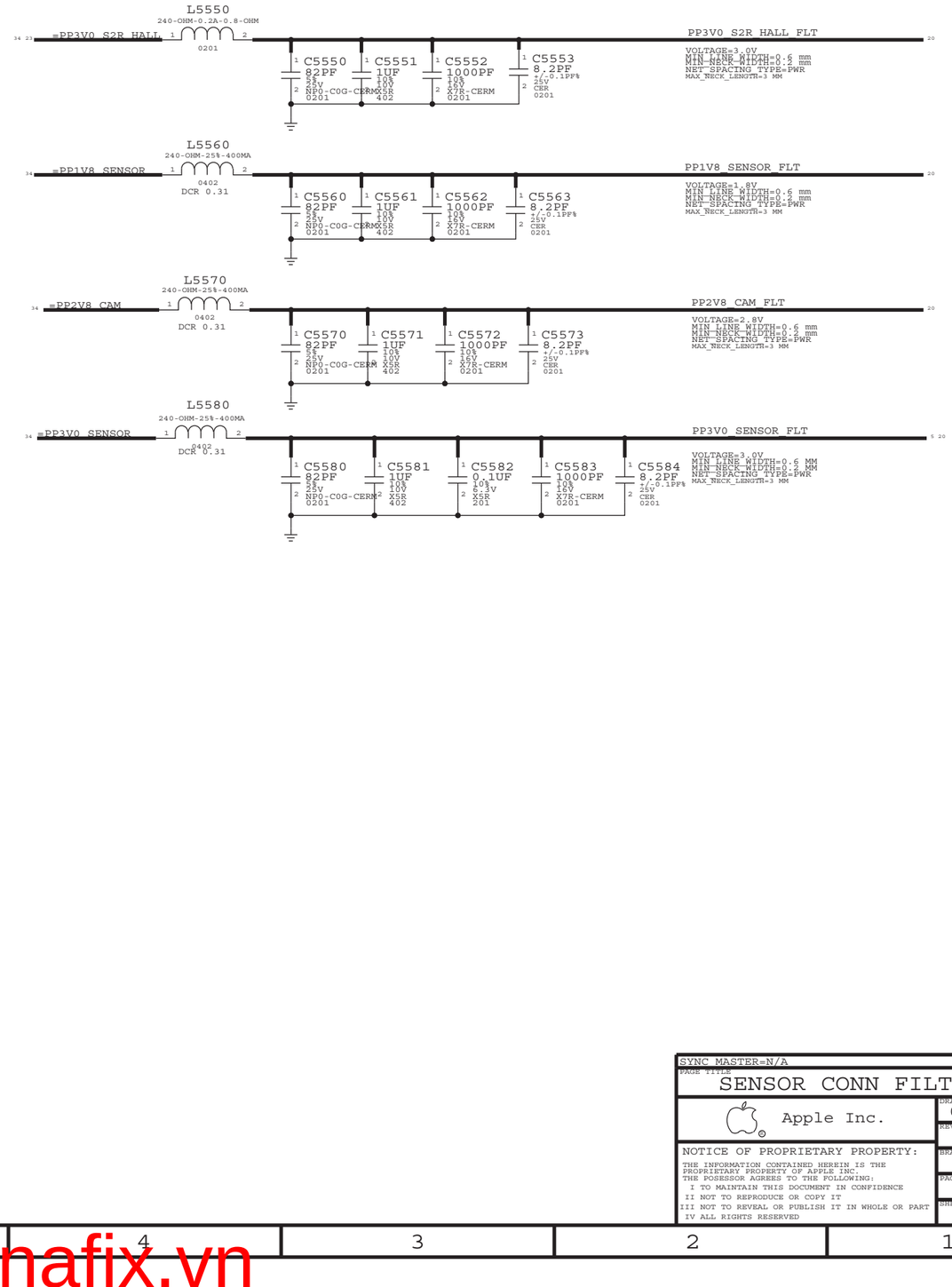
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SENSOR CONN FILTERS 1

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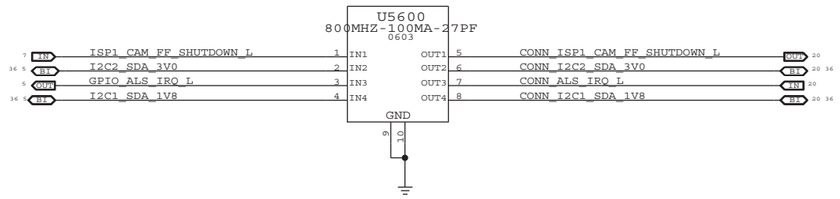
SHEET 21 OF 39

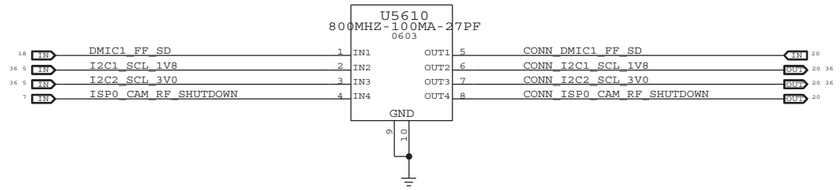
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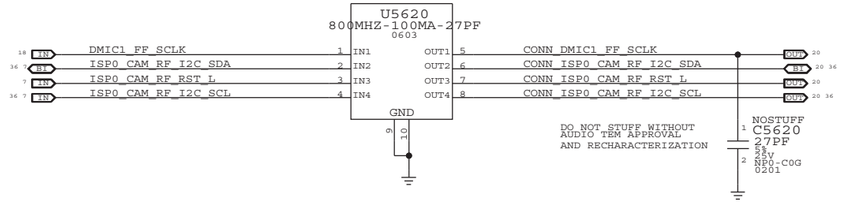
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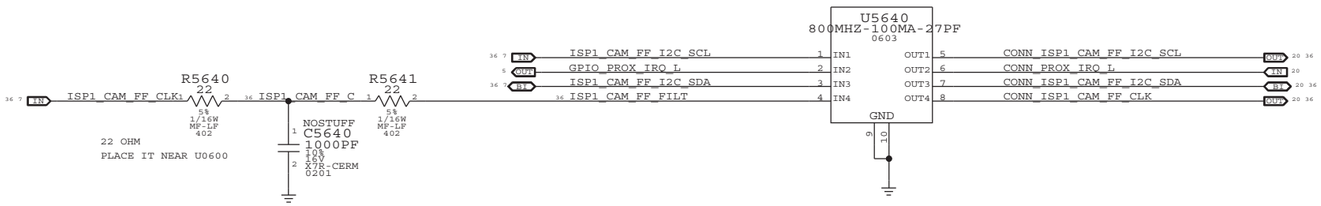
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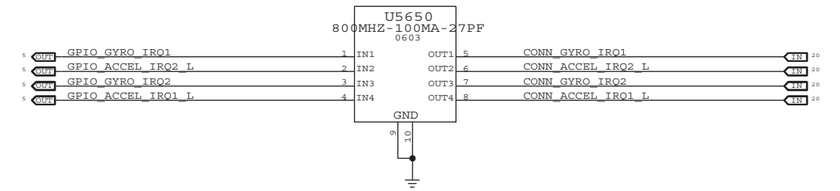
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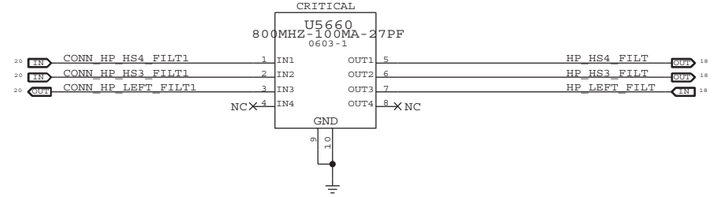


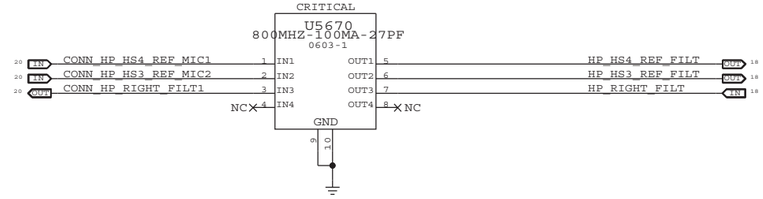












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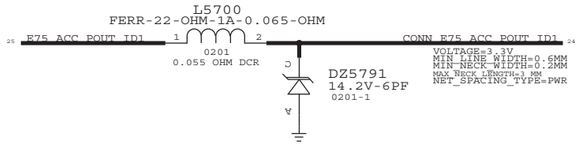
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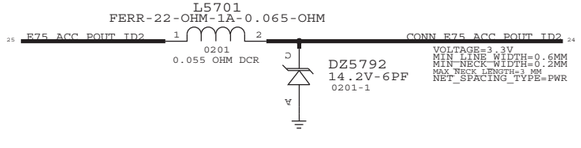
Apple Inc.

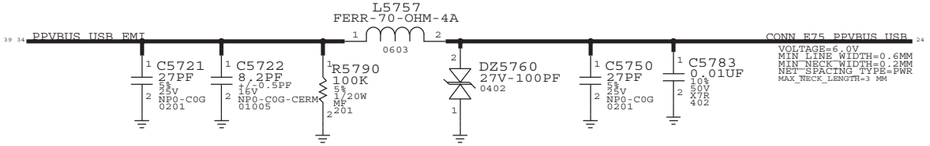
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REVISION A.0.0
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PAGE 56 OF 154
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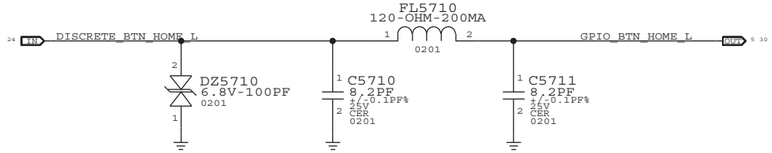
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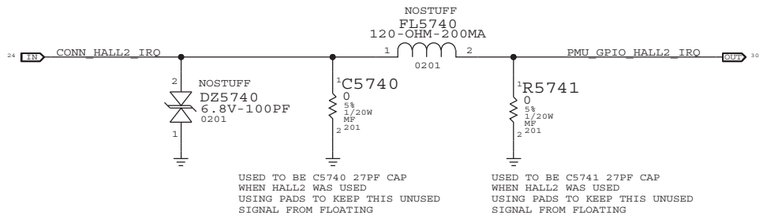


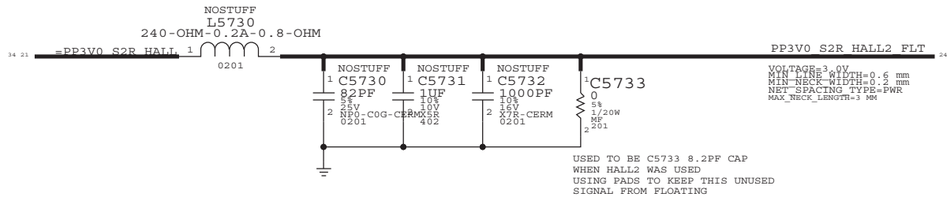




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155S0657	155S0537		FL5710,FL5750	
155S0741	155S0397		L5757	RDAR://PROBLEM/11238851







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E75 DOCK SUPPORT

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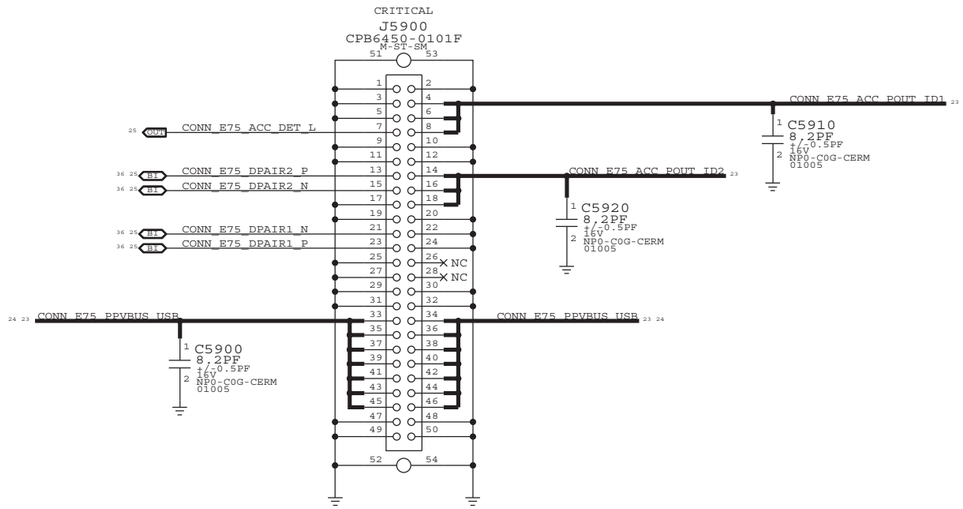
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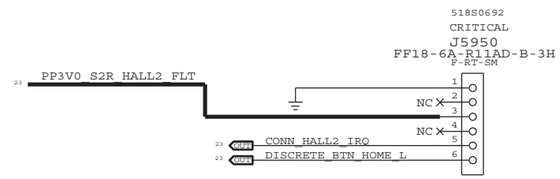
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IO FLEX CONNECTOR

PN 516S0542 (PLUG - MALE)





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TRISTAR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0614	1	IC,ASIC,TRISTAR,CBTL1608,A1,WLCSP36	U5900	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0773	155S0453	?	FL5990	RDAR://PROBLEM/10882925

TRISTAR BASEBAND USB MUX (NEEDED FOR MDM9600 BB)

BASEBAND USB MUX BYPASS

NOTE: ISOLATE SELECT SIGNAL FROM PMU ON MLB_B AND MLB_C SO THE MUX IS PERMANENTLY POINTED TO THE DOCK

SEL	Y+	Y-
0	M+	M-
1	D+	D-

DEFAULT =>

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Apple Inc.	DRAWING NUMBER: 051-9385	SIZE: D
	REVISION: A.0.0	
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CELLULAR/GPS HOTBAR PADS

OMIT

998-3732

J6000

HOT-BAR-PADS

H8-SM

5	IN	BB_JTAG_TMS_RF	1
			2
34	=BATT_POS_F_3G		3
			4
			5
			6
			7
			8
			9
27	IN	WLAN_TX_BLANK	10
39 30 25 4	OUT	RST_AP_L	11
5	IN	GPIO_BB_RADIO_ON_L	12
30	IN	PMU_GPIO_BB_PMU_RST_L	13
5	OUT	GPIO_BB_GSM_TXBURST	14
39 5	IN	GPIO_BB_RST_L	15
5	OUT	GPIO_BB_RESET_DET_L	16
			17
36 5	IN	GPIO_BB_HSIC_HOST_RDY	18
36 5	OUT	GPIO_BB_HSIC_RESUME	19
5	OUT	BB_JTAG_TDO_RF	20
5	IN	BB_JTAG_TDI_RF	21
5	IN	BB_JTAG_TRST_RF_L	22
5	OUT	GPIO_BB_GPS_SYNC	23
30	OUT	PMU_GPIO_BB_HOST_WAKE	24
			25
30	IN	BB_VBUS_DET	26
36 25	BI	USB_BBMUX_BB_P	27
36 25	BI	USB_BBMUX_BB_N	28
			29
36 25 5	OUT	UART1_BB_RXD	30
36 25 5	IN	UART1_BB_TXD	31
36 5	OUT	UART1_BB_CTS_L	32
36 5	IN	UART1_BB_RTS_L	33
			34
5	BI	GPIO_AP_MODEM_WAKE	35
36 5	OUT	GPIO_BB_HSIC_DEV_RDY	36
			37
36 26 4	BI	HSIC3_BB_STB	38
			39
36 26 4	BI	HSIC3_BB_DATA	40
			41
5	IN	BB_JTAG_TCK_RF	42

DEBUG

NOSTUFF

J6050

MM4829-2702

F-ST-SM

36 26 4 HSIC3_BB_STB — 1

NOSTUFF

J6051

MM4829-2702

F-ST-SM

36 26 4 HSIC3_BB_DATA — 1

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PAGE TITLE: CONNECTOR: CELLULAR	
Apple Inc.	DRAWING NUMBER: 051-9385 · SIZE: D
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WLAN/BT

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0171	1	WIFI MODULE - MURATA	U6101_RF	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0175	339S0171		U6101_RF	WIFI MODULE - USI
311S0548	311S0398		U6102_RF	

ANTENNA CONNECTOR

CRITICAL
J6190_RF
MM4829-2702
F-ST-SM

RF_ANT
WIFI 50S
50_OHM

CRITICAL
C6193_RF
3.9PF
+/-0.1PF
50V
NPO-CERM
0402

NOSTUFF
L6190_RF
5.6NH+/-0.3NH
0402

RF_ANT_MATCH1
WIFI 50S
50_OHM

CRITICAL
C6191_RF
0.2PF
+/-0.05PF
50V
NPO-CERM
0402

CONDUCTED TEST PORT

CRITICAL
J6191_RF
MM8030-2600RK0
F-ST-SM

RF_CAL
WIFI 50S
50_OHM

CRITICAL
C6192_RF
8.2PF
+/-0.25PF%
25V
NP0-C0G
0201

NOSTUFF
L6191_RF
5.6NH-3%-0.35A
0201

RF_CAL_MATCH
WIFI 50S
50_OHM

NOSTUFF
L6192_RF
5.6NH-3%-0.35A
0201

CRITICAL
U6104_RF
DPX205850DT-9038A1SJ
SM

XW6102_RF
SHORT-0402

34 BATT_VCC

C6101_RF
10UF
20%
6.3V
CERM-X5R
0402-1

C6102_RF
27PF
5%
16V
NP0-C0G
01005

33 BATT_VCC_WLAN

R6108_RF
0.00
0%
1/32W
MF
01005

13 PP_WLAN_VDDIO_1V8
VOLTAGE=1.8V

C6103_RF
0.01UF
10%
6.3V
X5R
01005

C6104_RF
27PF
5%
16V
NP0-C0G
01005

14 27 PP_WL_BT_VDDIO_AP
VOLTAGE=1.8V

NOSTUFF
R6105_RF
10K
5%
1/32W
MF
01005

R6107_RF
10K
5%
1/32W
MF
01005

15 VDDIO_1P8V
27 BATT_VCC
46 VBATT_RF_VCC
47 VBATT_RF_VCC

32K INTERFACE TO AP

XW6101_RF
SHORT-01005

14 CLK32K_AP — WLAN_CLK32K

32 CLK32K_AP
6 GPIO_6
29 VIN_1P2LDO
31 WL_REG_ON
30 BT_REG_ON
14 JTAG_SEL
28 SR_VLX
24 WLAN_HSIC_DATA
25 WLAN_HSIC_STROBE
40 RF_SW_CTRL_3

GPIO_6

WLAN_BUCK_OUT

27 14 IN WLAN_REG_ON

14 IN BT_REG_ON

JTAG_SEL

WLAN_SR_VLX1

27 14 50_HSIC_WLAN_DATA

27 14 50_HSIC_WLAN_STROBE

CRITICAL
L6111_RF
2.5UH-30%-0.7A-0.24OHM
0603

C6109
4.7UF
20%
6.3V
X5R-CERM1
402

R6109_RF
10K
5%
1/32W
MF
01005

NC
NO LONGER NEEDED BASED ON AND GATE REMOVAL

U6101_RF
LBEE5ZHTWC501
LGA
OMIT_TABLE

2G_ANT	42	18 50_WLAN_G	
5G_ANT	52	18 50_WLAN_A	
HOST_WAKE_BT	34	HOST_WAKE_BT	OUT 14
BT_WAKE	39	BT_WAKE	IN 14
BT_UART_RXD	38	BT_UART_RXD	IN 14
BT_UART_TXD	37	BT_UART_TXD	OUT 14
BT_UART_RTS*	35	BT_UART_RTS_L	OUT 14
BT_UART_CTS*	36	BT_UART_CTS_L	IN 14
BT_PCM_CLK	3	BT_PCM_CLK	B3 14
BT_PCM_SYNC	5	BT_PCM_SYNC	B3 14
BT_PCM_OUT	2	BT_PCM_OUT	OUT 14
BT_PCM_IN	4	BT_PCM_IN	IN 14
GPIO_0	9	HOST_WAKE_WLAN	OUT 14 27
GPIO_1	8	AP_HSIC3_RDY	IN 14 27
GPIO_2	10	WLAN_HSIC3_RESUME	1 PP6101_RF P4MM
GPIO_3	12	AGG_CHANNEL	27
GPIO_4	7	WLAN_UART_RXD	IN 14 27
GPIO_5	11	WLAN_UART_TXD	OUT 14 27
GPIO_12	13	HSIC_DEVICE_RDY	OUT 27

GND: 17 18 19 20 21 22 1 16 23 26 33 41 43 44 45 48 49 50 51

THRML_PAD: 53 54 55 56 57 58 59 60

CRITICAL
C6107_RF
8.2PF
+/-0.25PF%
25V
NP0-C0G
0201

18 50_WLAN_G_1

CRITICAL
C6108_RF
4.7PF
+/-0.1PF
25V
C0G-CERM
0201

18 50_WLAN_A_DIPLX

NOSTUFF
C6111_RF
0.2PF
+/-0.05PF
25V
C0G-CERM
201

R6111_RF
10K
5%
1/32W
MF
01005

PULL DOWN RESISTORS

GPIO6	SDIO_DATA<1>	SDIO_DATA<2>	MODE	DEFAULT ARM STATE
0	X	X	SDIO	IN RESET
1	X	0	GSPI	IN RESET
1	0	1	HSIC	OUT OF RESET
1	1	1	BOOTLESS HSIC	IN RESET

27 14 IN PP_WL_BT_VDDIO_AP

R6113_RF
10K
5%
1/32W
MF
01005

27 HSIC_DEVICE_RDY

U6102_RF
74AUP1G08GF
SOT891

R6112_RF
1.00M
1%
1/32W
MF
01005

27 14 IN WLAN_REG_ON — WLAN_REG_ON_RC

C6110_RF
0.22UF
20%
6.3V
X5R
0201

NC

DEV_HSIC3_RDY 14 27

R6114_RF
0.00
0%
1/32W
MF
01005

27 AGG_CHANNEL — WLAN_TX_BLANK OUT 26

27 14 WLAN_REG_ON — PP6102_RF P4MM
27 14 HOST_WAKE_WLAN — PP6103_RF P4MM
27 14 AP_HSIC3_RDY — PP6104_RF P4MM
27 14 DEV_HSIC3_RDY — PP6105_RF P4MM
27 14 WLAN_UART_RXD — PP6106_RF P4MM
27 14 WLAN_UART_TXD — PP6107_RF P4MM

27 AGG_CHANNEL — PP6109_RF P4MM
27 14 50_HSIC_WLAN_DATA — PP6110_RF P4MM
27 14 50_HSIC_WLAN_STROBE — PP6111_RF P4MM
27 HSIC_DEVICE_RDY — PP6112_RF P4MM

CHANGE LIST

07FEB2012 MUSHTAQ COPIED FROM N41, ADDED J2 ANT MATCH/CONN
C6107 FROM 20PF TO 8.2PF, C6108 FROM 10PF TO 4.7PF
U6104 FROM SOSHIN TO MURATA LFD212G45DS5D355

13FEB2012 AMANDA CHANGED OMIT TO OMIT_TABLE AND UPDATED
BOM OPTION TABLES TO ALTERNATE TABLES
REMOVED BOM TABLE FOR C6111_RF (NOW ALWAYS NOSTUFF)

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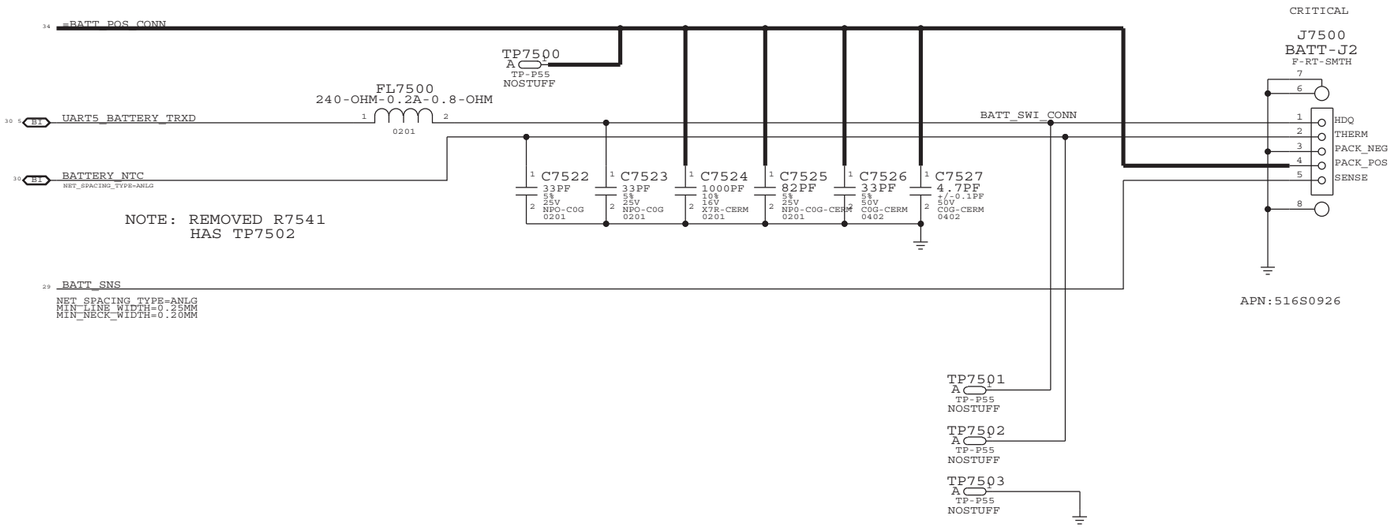
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0274	?		RDAR://PROBLEM/11282371

FL7500,L3620,L5550,L5730



APN:516S0926

SYNC MASTER=MADHAVI SYNC DATE=12/06/2011

PAGE TITLE

POWER: BATTERY CONNECTOR

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VCC MAIN BYPASS

TOTAL CAPS = ~400UF

PLACE ONE 10UF CAP AT EACH VDD INPUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND,1.0UH,20%,59MO,2.74A	L8100,L8101,L8102,L8103,L8109,L8110	CRITICAL	
152S1638	1	IND,1.0UH,20%,64MO,2.3A	L8104	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?	?	

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0339	128S0279	?	C8165,C8166	RDAR://PROBLEM/8967213
197S0399	197S0392	?	Y8138	RDAR://PROBLEM/9936684

USB REVERSE VOLTAGE PROTECTION

LDO BYPASS

NOTE: FOR NO BATTERY SITUATION

SYNC_MASTER=MADHAVI SYNC_DATE=12/06/2011

PAGE TITLE: PMU: ADRIANA PAGE 1

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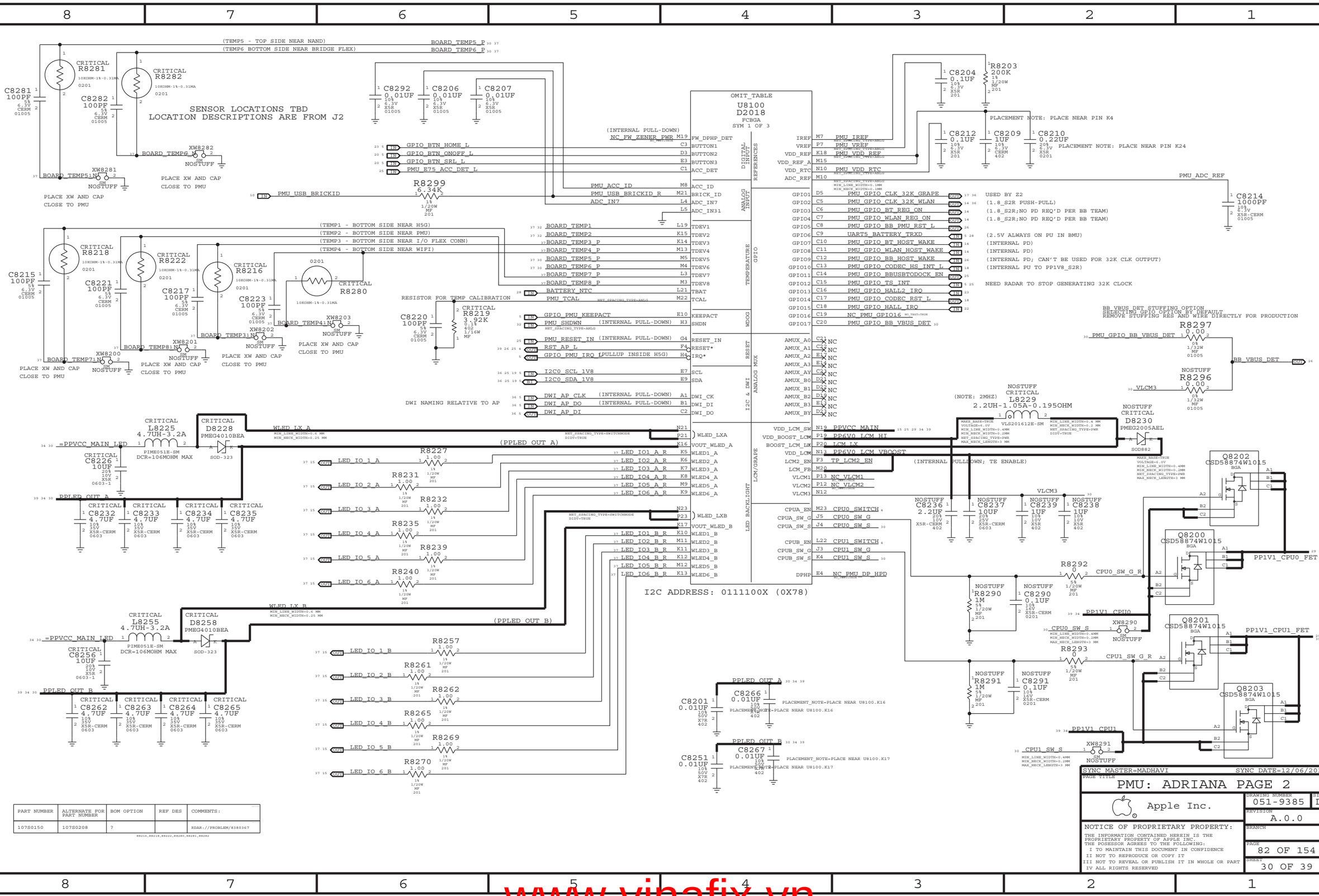
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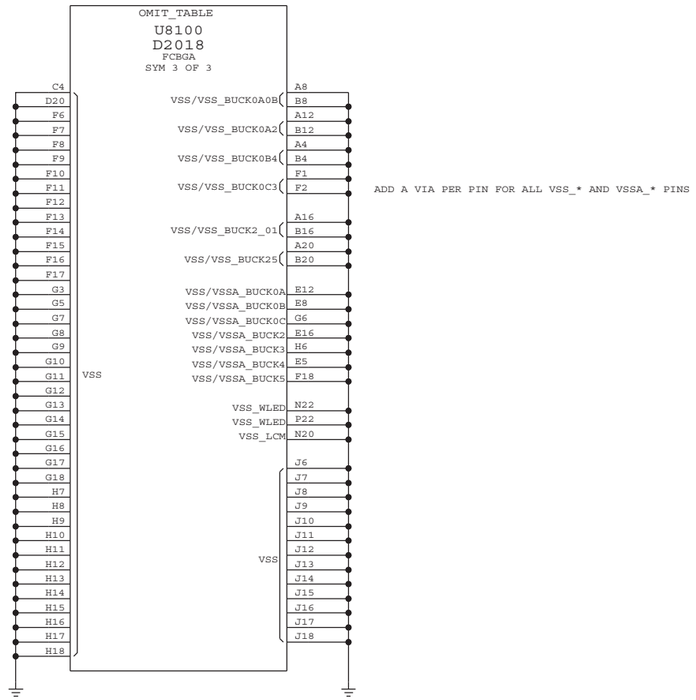
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	?		RDAR://PROBLEM/8380367

R8216,R8218,R8222,R8280,R8281,R8282

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SYNC MASTER=MADHAVI SYNC DATE=12/06/2011

PAGE TITLE

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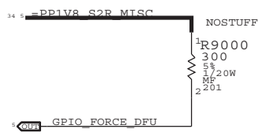
SHEET 31 OF 39

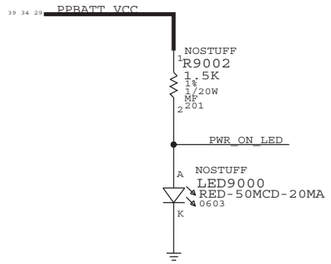
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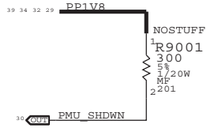
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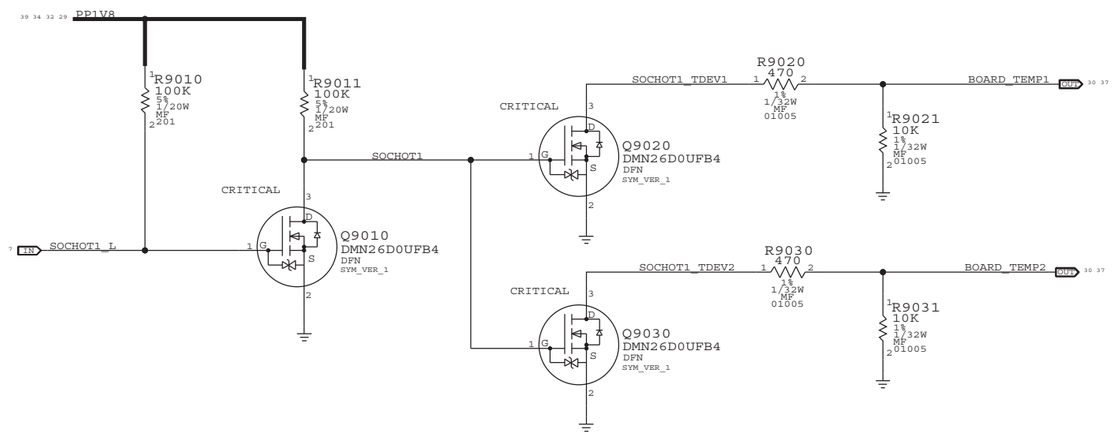
DEBUG RESET ACCESS







SOCHOT TO PMU TDEV1/TDEV2



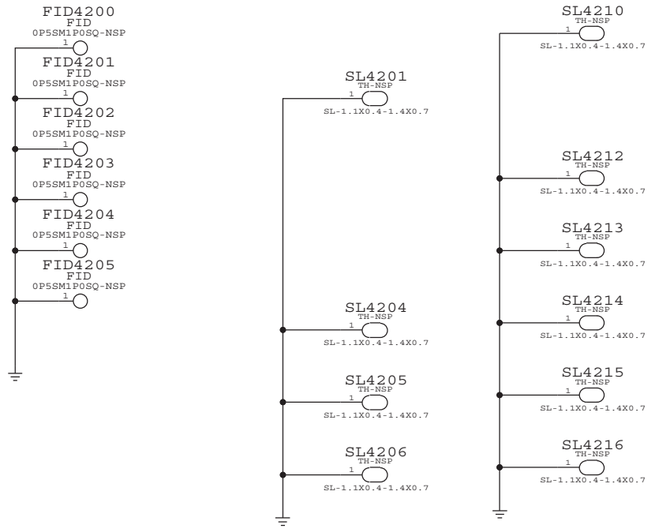
SYNC_MASTER=MLB	SYNC_DATE=11/09/2011
PAGE TITLE: DEBUG/MISC.	
Apple Inc.	DRAWING NUMBER: 051-9385 SIZE: D
	REVISION: A.0.0
	BRANCH:
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PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



SYNC MASTER=N/A SYNC DATE=N/A

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TEST/HOLES/FIDUCUALS

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POWER CONNECTIONS

BUCK0A

39 30 PP1V1_CPU0 = =PPVDD_CPU0_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK0B

39 30 PP1V1_CPU1 = =PPVDD_CPU1_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK0C

39 29 PP1V1_CPUB = =PPVDD_CPUB_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK2

39 29 PP1V2_SOC = =PPVDD_SOC_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK3

39 29 PP1V8_S2R = =PP1V8_S2R_MISC 6 32
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= VDDIO_WLAN_BT_1V8 14
= =PP1V8_S2R_USBMUX 25
= =PP1V8_S2R_DDR 11 12

BUCK4

39 29 PP1V2_S2R = =PP1V2_S2R_H5 8
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V2_S2R_DDR 11 12

BUCK3_SW

CPU1V8_SW

32 29 39 PP1V8 = =PP1V8_SENSOR 21
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3MM
= =PP1V8_AUDIO 18
= =PP1V8_VDDIO18_H5 4 6 7 9
= =PP1V8_H5 4 5 7 10
= =PP1V8_MIPI_H5 7
= =PP1V8_DP_H5 7
= =PP1V8_EDP_H5 7
= =PP1V8_NAND_H5 6 9
= =PP1V8_NAND 13
= =PP1V8_PLL_H5 4
= =PP1V8_MISC 16

BUCK4_SW

CPU1V2_SW

39 29 PP1V2 = =PP1V2_VDDQ_DDR 11 12
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V2_VDDIOD_H5 8 9
= =PP1V2_HSIC_H5 4

BUCK5

39 29 PP3V3_OUT = =PP3V3_NAND 13
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V3_USB_H5 4
= =PP3V3_LCD 15

BACKLIGHT BOOST

39 30 PPLED_OUT_A = =PPLED_REG_A 15
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

39 30 PPLED_OUT_B = =PPLED_REG_B 15
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO1

39 29 PP3V0_GRAPE = =PP3V0_GRAPE 16 17
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_GRAPE_MARIO1 16
= =PP3V0_GRAPE_Z1 17
= =PP3V0_GRAPE_Z2 17

LDO2

39 29 19 PP1V7_VA_VCP = =PP1V7_VA_VCP 18 19
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO3 (NO LONGER NEEDED)

39 29 PP3V2_S2R_USBMUX = =PP3V2_S2R_USBMUX 25
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO4

39 29 PP3V0_SENSOR = =PP3V0_SENSOR 21
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO6

39 29 PP3V3_ACC = =PP3V3_ACC 25
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO7

29 PP3V0_S2R_TRISTAR = =PP3V0_S2R_TRISTAR 25
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO8

39 29 PP3V0_S2R_HALL = =PP3V0_S2R_HALL 21 23
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO9

39 29 PP3V0_IO = =PP3V0_VDDIO30_H5 9
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO11

39 29 PP2V8_CAM = =PP2V8_CAM 21
MAKE_BASE=TRUE
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO12

39 29 PP1V0 = =PP1V0_MIPI_H5 7
MAKE_BASE=TRUE
VOLTAGE=1.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V0_DP_PAD_DVDD_H5 7
= =PP1V0_EDP_PAD_DVDD_H5 7
= =PP1V0_USB_H5 4
= =PP1V0_HSIC_H5 4
= =PP1V0_MIPI_PLL_H5 7

LDO16

39 29 PP1V1_SRAM = =PPVDD_SRAM_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

39 29 PP1V8_ALWAYS = =PP1V8_ALWAYS 5
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

CHARGER MAIN

39 30 29 25 15 PPVCC_MAIN = =PPVCC_MAIN_AUDIO 18 19
MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PPVCC_MAIN_LED 30
= =PPVCC_MAIN_CPU0 29
= =PPVCC_MAIN_CPU1 29
= =PPVCC_MAIN_SOC 29

BATTERY

39 32 29 PPBATT_VCC = =BATT_POS_CONN 28
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =BATT_POS_F_3G 24 CELLULAR RADIO
= =BATT_VCC 27 WLAN

USB POWER INPUT

39 23 PPVBUS_USB_EMI = =PPVBUS_USB_DCIN 29
MAKE_BASE=TRUE
VOLTAGE=6V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
POWER ALIASES

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA,BGA06-06,BGA_P4	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	3.0 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL2,ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL3,ISL8	Y	0.065 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4,ISL7	Y	0.053 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL5	Y	0.072 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL6	Y	0.059 MM	0.055 MM	3.0 MM		

90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
90_OHM_DIFF	ISL2,ISL9	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL3,ISL8	Y	0.062 MM	0.052 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL4,ISL7	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL5,ISL6	Y	0.052 MM	0.052 MM	=STANDARD	0.105 MM	0.105 MM

DDR 45 OHMS SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_45_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.105 MM	3.0 MM		
DDR_45_OHM_SE	ISL2	Y	0.055 MM	0.055 MM	3.0 MM		
DDR_45_OHM_SE	ISL3	Y	0.065 MM	0.065 MM	3.0 MM		
DDR_45_OHM_SE	ISL4	Y	0.053 MM	0.053 MM	3.0 MM		
DDR_45_OHM_SE	ISL5,ISL6	Y	0.072 MM	0.072 MM	3.0 MM		
DDR_45_OHM_SE	*	N	0.055 MM	0.055 MM	3.0 MM		

DDR 90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_90_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
DDR_90_OHM_DIFF	ISL2	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL3	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL4	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL5,ISL6	Y	0.066 MM	0.066 MM	=STANDARD	0.180 MM	0.180 MM
DDR_90_OHM_DIFF	*	N	0.056 MM	0.056 MM	=STANDARD	0.180 MM	0.180 MM

WIFI PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WIFI_50S	TOP,BOTTOM	Y	0.245 MM	0.2 MM	=STANDARD		
WIFI_50S	*	N	=STANDARD	=STANDARD	=STANDARD		
WIFI_PWR100	*	Y	0.10 MM	0.050 MM	=STANDARD		
WIFI_PWR1000	*	Y	1.00 MM	0.100 MM	=STANDARD		

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.5 MM	0.20 MM	10 MM	0.10 MM	0.10 MM
AUDIO_DIFF	*	Y	0.1 MM	0.09 MM	10 MM	0.10 MM	0.10 MM
LED	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM
TEMP_SENSE	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

TCF VERSION (USING SPACING RULE)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TCF_VERSION	*	0.104 MM	?

0.104 - 11/30/2011

TCF_VERSION NC_UARTS_TXD *ASSIGNING RULE TO NC NET

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?
BGA_P4_SPA	*	0.200 MM	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.050 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.075 MM	?
2:1_SPACING	*	0.100 MM	?
2.5:1_SPACING	*	0.125 MM	?
3:1_SPACING	*	0.150 MM	?
4:1_SPACING	*	0.200 MM	?
5:1_SPACING	*	0.250 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?
0P2_SPACING	*	0.20 MM	?

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	
GND_P1SPACING	*	0.1 MM	
SWITCHNODE	*	0.2 MM	

POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.20 MM	3.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	3.0 MM		
PWR_PMU	*	Y	0.6MM	0.20 MM	3.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
*	*	BGA_P4	BGA_P4_SPA

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

SYNC MASTER=MIKE SYNC DATE=11/30/2011

PAGE TITLE
CONSTRAINTS: MLB RULES

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	CLK_50S	CLK	PMU_GPIO_CLK_32K_GRAPE
	CLK_50S	CLK	PMU_GPIO_CLK_32K_WLAN
	CLK_50S	CLK	ISP1_CAM_FF_CLK
	CLK_50S	CLK	CONN_ISP1_CAM_FF_CLK
	CLK_50S	CLK	ISP0_CAM_RF_CLK
	CLK_50S	CLK	CONN_ISP0_CAM_RF_CLK
	I2S_50S	I2S	I2S0_CODEC_ASP_MCK
	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R
	CLK_50S	CLK	ISP0_CAM_RF_CLK_R
	CLK_50S	CLK	ISP1_CAM_FF_CLK_R
	CLK_50S	CLK	ISP1_CAM_FF_C
	CLK_50S	CLK	ISP0_CAM_RF_C
	CLK_50S	CLK	ISP1_CAM_FF_FILT
	CLK_50S	CLK	ISP0_CAM_RF_FILT

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	UART_50S	UART	UART2_TS_ACC_RXD
	UART_50S	UART	UART2_TS_ACC_TXD
	UART_50S	UART	UART4_WLAN_RXD
	UART_50S	UART	UART4_WLAN_TXD
	UART_50S	UART	UART1_BB_CTS_L
	UART_50S	UART	UART1_BB_RTS_L
	UART_50S	UART	UART1_BB_TXD
	UART_50S	UART	UART1_BB_RXD
	UART_50S	UART	UART3_BT_CTS_L
	UART_50S	UART	UART3_BT_RTS_L
	UART_50S	UART	UART3_BT_RXD
	UART_50S	UART	UART3_BT_TXD
	UART_50S	UART	UART6_AP_RXD
	UART_50S	UART	UART6_AP_TXD

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	SPI_50S	SPI	SPI3_GRAPE_MISO
	SPI_50S	SPI	SPI3_GRAPE_MOSI
	SPI_50S	SPI	SPI3_GRAPE_SCLK
	SPI_50S	SPI	SPI3_GRAPE_CS_L
	SPI_50S	SPI	SPI2_IPC_MISO
	SPI_50S	SPI	SPI2_IPC_MOSI
	SPI_50S	SPI	SPI2_IPC_SCLK
	SPI_50S	SPI	GPIO_BB_HSIC_RESUME
	SPI_50S	SPI	SPI1_CODEC_MISO
	SPI_50S	SPI	SPI1_CODEC_MOSI
	SPI_50S	SPI	SPI1_CODEC_SCLK
	SPI_50S	SPI	SPI1_CODEC_CS_L

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
		DWI	DWI_AP_CLK
		DWI	DWI_AP_DI
		DWI	DWI_AP_DO

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
		JTAG	JTAG_AP_TCK
		JTAG	JTAG_AP_TMS
		JTAG	JTAG_AP_TDI
		JTAG	TP_JTAG_AP_TDO
		RST	JTAG_AP_TRST_L

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	I2C_50S	I2C	I2C1_SDA_1V8
	I2C_50S	I2C	I2C1_SCL_1V8
	I2C_50S	I2C	I2C0_SDA_1V8
	I2C_50S	I2C	I2C0_SCL_1V8
	I2C_50S	I2C	I2C2_SDA_3V0
	I2C_50S	I2C	I2C2_SCL_3V0
	I2C_50S	I2C	ISP0_CAM_RF_I2C_SCL
	I2C_50S	I2C	ISP0_CAM_RF_I2C_SDA
	I2C_50S	I2C	ISP1_CAM_FF_I2C_SCL
	I2C_50S	I2C	ISP1_CAM_FF_I2C_SDA
	I2C_50S	I2C	CONN_I2C1_SDA_1V8
	I2C_50S	I2C	CONN_I2C1_SCL_1V8
	I2C_50S	I2C	CONN_I2C2_SCL_3V0
	I2C_50S	I2C	CONN_I2C2_SDA_3V0
	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SCL
	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SDA
	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SCL
	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SDA

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
		CRYSTAL	XTAL_AP_24M_I
		CRYSTAL	XTAL_AP_24M_O
		CRYSTAL	AP_24M_O
		CRYSTAL	PMU_XTAL
		CRYSTAL	PMU_EXTAL

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	I2S_50S	I2S	I2S0_CODEC_ASP_BCLK
	I2S_50S	I2S	I2S0_CODEC_ASP_LRCK
	I2S_50S	I2S	I2S0_CODEC_ASP_DIN
	I2S_50S	I2S	I2S0_CODEC_ASP_DOUT
	I2S_50S	I2S	I2S0_CODEC_ASP_SDOUT
	I2S_50S	I2S	I2S0_CODEC_ASP_MCK
	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R
	I2S_50S	I2S	I2S3_CODEC_XSP_BCLK
	I2S_50S	I2S	I2S3_CODEC_XSP_LRCK
	I2S_50S	I2S	I2S3_CODEC_XSP_DIN
	I2S_50S	I2S	I2S3_CODEC_XSP_DOUT
	I2S_50S	I2S	I2S0_CODEC_XSP_SDOUT
	I2S_50S	I2S	I2S2_BT_BCLK
	I2S_50S	I2S	I2S2_BT_LRCK
	I2S_50S	I2S	I2S2_BT_DIN
	I2S_50S	I2S	I2S2_BT_DOUT

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	USB_90D	USB	USB_AP_P
	USB_90D	USB	USB_AP_N
	USB_90D	USB	USB_BBMUX_BB_P
	USB_90D	USB	USB_BBMUX_BB_N
	USB_90D	USB	USB_TS_BBMUX_P
	USB_90D	USB	USB_TS_BBMUX_N
	USB_90D	USB	USB11_AP_BBMUX_P
	USB_90D	USB	USB11_AP_BBMUX_N
	USB_90D	USB	CONN_E75_DPAIR1_P
	USB_90D	USB	CONN_E75_DPAIR1_N
	USB_90D	USB	CONN_E75_DPAIR2_P
	USB_90D	USB	CONN_E75_DPAIR2_N
	USB_90D	USB	TS_E75_DPAIR1_P
	USB_90D	USB	TS_E75_DPAIR1_N
	USB_90D	USB	TS_E75_DPAIR2_P
	USB_90D	USB	TS_E75_DPAIR2_N

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC_RDY	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	HSIC	HSIC	HSIC3_BB_DATA
	HSIC	HSIC	HSIC3_BB_STB
	HSIC	HSIC	HSIC1_WLAN_DATA
	HSIC	HSIC	HSIC1_WLAN_STB
	HSIC	HSIC_RDY	GPIO_BB_HSIC_DEV_RDY
	HSIC	HSIC_RDY	GPIO_BB_HSIC_HOST_RDY
	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY
	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY
	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_DEV_RDY

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MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI0C	*	*	4:1_SPACING
MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J11A	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_P	7 21
J11B	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_N	7 21
J11C	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<0>	7 21
J12A	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<0>	7 21
J12B	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<1>	7 21
J12C	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<1>	7 21
J13A	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_P	20 21
J13B	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_N	20 21
J13C	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<0>	20 21
J14A	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<0>	20 21
J14B	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<1>	20 21
J14C	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<1>	20 21
J15A	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_P	7 21
J15B	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_N	7 21
J15C	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_P<0>	7 21
J16A	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_N<0>	7 21
J16B	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_P	20 21
J16C	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_N	20 21
J17A	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_P<0>	20 21
J17B	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_N<0>	20 21

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E584	AUDIO_DIFF	AUDIO	HP_MIC_P	18
E585	AUDIO_DIFF	AUDIO	HP_MIC_N	18
E587	AUDIO_DIFF	AUDIO	L81_AIN2_P	18
E586	AUDIO_DIFF	AUDIO	L81_AIN2_N	18
E588	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N_FILT	19
E589	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P_FILT	19
E591	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N	19
E590	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P	19
E592	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N_FILT	19
E593	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P_FILT	19
E595	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N	19
E594	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P	19
E597	SPEAKER	AUDIO	SPKR_L_P	19
E596	SPEAKER	AUDIO	SPKR_L_N	19
E598	SPEAKER	AUDIO	SPKR_L_CONN_P	19
E599	SPEAKER	AUDIO	SPKR_L_CONN_N	19
E602	SPEAKER	AUDIO	SPKR_R_P	19
E601	SPEAKER	AUDIO	SPKR_R_N	19
E608	SPEAKER	AUDIO	SPKR_R_CONN_P	19
E607	SPEAKER	AUDIO	SPKR_R_CONN_N	19
E610	SPEAKER	AUDIO	SPKR_L_FLR	19
E611	SPEAKER	AUDIO	SPKR_R_FLR	19
E644	AUDIO_DIFF	AUDIO	SPKR_L_SES_N	19
E645	AUDIO_DIFF	AUDIO	SPKR_L_SES_P	19
E646	AUDIO_DIFF	AUDIO	SPKR_R_SES_N	19
E647	AUDIO_DIFF	AUDIO	SPKR_R_SES_P	19
E648	USB_90D	USB	MIKEY_TS_P	18 25
E649	USB_90D	USB	MIKEY_TS_N	18 25
E600	USB_90D	USB	L81_MBUS_P	18
E603	USB_90D	USB	L81_MBUS_N	18

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E630	EDP_90D	EDP	EDP_AUX_P	7 15
E631	EDP_90D	EDP	EDP_AUX_N	7 15
E633	EDP_50S	EDP	EDP_HPD	7 15
E634	EDP_90D	EDP	EDP_DATA_P<0>	7 15
E636	EDP_90D	EDP	EDP_DATA_N<0>	7 15
E635	EDP_90D	EDP	EDP_DATA_P<1>	7 15
E637	EDP_90D	EDP	EDP_DATA_N<1>	7 15
E638	EDP_90D	EDP	EDP_DATA_P<2>	7 15
E639	EDP_90D	EDP	EDP_DATA_N<2>	7 15
E641	EDP_90D	EDP	EDP_DATA_P<3>	7 15
E640	EDP_90D	EDP	EDP_DATA_N<3>	7 15
E642	EDP_90D	EDP	EDP_AUX_EMI_P	15
E643	EDP_90D	EDP	EDP_AUX_EMI_N	15
E645	EDP_90D	EDP	EDP_DATA_EMI_P<0>	15
E644	EDP_90D	EDP	EDP_DATA_EMI_N<0>	15
E646	EDP_90D	EDP	EDP_DATA_EMI_P<1>	15
E647	EDP_90D	EDP	EDP_DATA_EMI_N<1>	15
E648	EDP_90D	EDP	EDP_DATA_EMI_P<2>	15
E649	EDP_90D	EDP	EDP_DATA_EMI_N<2>	15
E651	EDP_90D	EDP	EDP_DATA_EMI_P<3>	15
E650	EDP_90D	EDP	EDP_DATA_EMI_N<3>	15
E652	EDP_90D	EDP	CONN_EDP_AUX_EMI_P	15
E653	EDP_90D	EDP	CONN_EDP_AUX_EMI_N	15
E654	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<0>	15
E655	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<0>	15
E656	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<1>	15
E657	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<1>	15
E658	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<2>	15
E659	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<2>	15
E661	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<3>	15
E660	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<3>	15

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	3:1_SPACING
LEDB	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E681	LED	LEDA	LED_IO1_A_R	30
E682	LED	LEDB	LED_IO1_B_R	30
E683	LED	LEDA	LED_IO2_A_R	30
E684	LED	LEDB	LED_IO2_B_R	30
E685	LED	LEDA	LED_IO3_A_R	30
E686	LED	LEDB	LED_IO3_B_R	30
E687	LED	LEDA	LED_IO4_A_R	30
E688	LED	LEDB	LED_IO4_B_R	30
E689	LED	LEDA	LED_IO5_A_R	30
E691	LED	LEDB	LED_IO5_B_R	30
E692	LED	LEDA	LED_IO6_A_R	30
E693	LED	LEDB	LED_IO6_B_R	30
E694	LED	LEDA	LED_IO_1_A	15 30
E695	LED	LEDB	LED_IO_1_B	15 30
E696	LED	LEDA	LED_IO_2_A	15 30
E697	LED	LEDB	LED_IO_2_B	15 30
E698	LED	LEDA	LED_IO_3_A	15 30
E699	LED	LEDB	LED_IO_3_B	15 30
E700	LED	LEDA	LED_IO_4_A	15 30
E701	LED	LEDB	LED_IO_4_B	15 30
E702	LED	LEDA	LED_IO_5_A	15 30
E704	LED	LEDB	LED_IO_5_B	15 30
E705	LED	LEDA	LED_IO_6_A	15 30
E706	LED	LEDB	LED_IO_6_B	15 30

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
BOARD_TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E670		BOARD_TEMP	BOARD_TEMP1	30 32
E671		BOARD_TEMP	BOARD_TEMP2	30 32
E690	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_P	30
E703	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_N	30
E708	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_P	30
E709	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_N	30
E710	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_P	30
E711	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_N	30
E712	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_P	30
E713	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_N	30
E602	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_P	30
E603	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_N	30
E604	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_P	30
E605	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_N	30

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DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DDR_45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DDR_90_OHM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DDR_50S	DDR	DDR0_CA<9..0>	8 11
	DDR_50S	DDR	DDR0_DM<3..0>	8 11
	DDR_90D	DDR	DDR0_CK_P	8 11
	DDR_90D	DDR	DDR0_CK_N	8 11
	DDR_50S	DDR	DDR0_CKE<1..0>	8 11
	DDR_50S	DDR	DDR0_CSN<2..0>	8 11
	DDR_50S	DDR	DDR0_ZQ	11
	DDR_50S	DDR	DDR0_DQ<7..0>	8 11
	DDR_90D	DDR	DDR0_DQS_P<0>	8 11
	DDR_90D	DDR	DDR0_DQS_N<0>	8 11
	DDR_50S	DDR	DDR0_DQ<15..8>	8 11
	DDR_90D	DDR	DDR0_DQS_P<1>	8 11
	DDR_90D	DDR	DDR0_DQS_N<1>	8 11
	DDR_50S	DDR	DDR0_DQ<23..16>	8 11
	DDR_90D	DDR	DDR0_DQS_P<2>	8 11
	DDR_90D	DDR	DDR0_DQS_N<2>	8 11
	DDR_50S	DDR	DDR0_DQ<31..24>	8 11
	DDR_90D	DDR	DDR0_DQS_P<3>	8 11
	DDR_90D	DDR	DDR0_DQS_N<3>	8 11
	DDR_50S	DDR	DDR1_CA<9..0>	8 11
	DDR_50S	DDR	DDR1_DM<3..0>	8 11
	DDR_90D	DDR	DDR1_CK_P	8 11
	DDR_90D	DDR	DDR1_CK_N	8 11
	DDR_50S	DDR	DDR1_CKE<1..0>	8 11
	DDR_50S	DDR	DDR1_CSN<2..0>	8 11
	DDR_50S	DDR	DDR1_ZQ	11
	DDR_50S	DDR	DDR1_DQ<7..0>	8 11
	DDR_90D	DDR	DDR1_DQS_P<0>	8 11
	DDR_90D	DDR	DDR1_DQS_N<0>	8 11
	DDR_50S	DDR	DDR1_DQ<15..8>	8 11
	DDR_90D	DDR	DDR1_DQS_P<1>	8 11
	DDR_90D	DDR	DDR1_DQS_N<1>	8 11
	DDR_50S	DDR	DDR1_DQ<23..16>	8 11
	DDR_90D	DDR	DDR1_DQS_P<2>	8 11
	DDR_90D	DDR	DDR1_DQS_N<2>	8 11
	DDR_50S	DDR	DDR1_DQ<31..24>	8 11
	DDR_90D	DDR	DDR1_DQS_P<3>	8 11
	DDR_90D	DDR	DDR1_DQS_N<3>	8 11
	DDR_50S	DDR	DDR2_CA<9..0>	8 12
	DDR_50S	DDR	DDR2_DM<3..0>	8 12
	DDR_90D	DDR	DDR2_CK_P	8 12
	DDR_90D	DDR	DDR2_CK_N	8 12
	DDR_50S	DDR	DDR2_CKE<1..0>	8 12
	DDR_50S	DDR	DDR2_CSN<2..0>	8 12
	DDR_50S	DDR	DDR2_ZQ	12
	DDR_50S	DDR	DDR2_DQ<7..0>	8 12
	DDR_90D	DDR	DDR2_DQS_P<0>	8 12
	DDR_90D	DDR	DDR2_DQS_N<0>	8 12
	DDR_50S	DDR	DDR2_DQ<15..8>	8 12
	DDR_90D	DDR	DDR2_DQS_P<1>	8 12
	DDR_90D	DDR	DDR2_DQS_N<1>	8 12
	DDR_50S	DDR	DDR2_DQ<23..16>	8 12
	DDR_90D	DDR	DDR2_DQS_P<2>	8 12
	DDR_90D	DDR	DDR2_DQS_N<2>	8 12
	DDR_50S	DDR	DDR2_DQ<31..24>	8 12
	DDR_90D	DDR	DDR2_DQS_P<3>	8 12
	DDR_90D	DDR	DDR2_DQS_N<3>	8 12
	DDR_50S	DDR	DDR3_CA<9..0>	8 12
	DDR_50S	DDR	DDR3_DM<3..0>	8 12
	DDR_90D	DDR	DDR3_CK_P	8 12
	DDR_90D	DDR	DDR3_CK_N	8 12
	DDR_50S	DDR	DDR3_CKE<1..0>	8 12
	DDR_50S	DDR	DDR3_CSN<2..0>	8 12
	DDR_50S	DDR	DDR3_ZQ	12
	DDR_50S	DDR	DDR3_DQ<7..0>	8 12
	DDR_90D	DDR	DDR3_DQS_P<0>	8 12
	DDR_90D	DDR	DDR3_DQS_N<0>	8 12
	DDR_50S	DDR	DDR3_DQ<15..8>	8 12
	DDR_90D	DDR	DDR3_DQS_P<1>	8 12
	DDR_90D	DDR	DDR3_DQS_N<1>	8 12
	DDR_50S	DDR	DDR3_DQ<23..16>	8 12
	DDR_90D	DDR	DDR3_DQS_P<2>	8 12
	DDR_90D	DDR	DDR3_DQS_N<2>	8 12
	DDR_50S	DDR	DDR3_DQ<31..24>	8 12
	DDR_90D	DDR	DDR3_DQS_P<3>	8 12
	DDR_90D	DDR	DDR3_DQS_N<3>	8 12

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND0	*	*	2:1_SPACING
NAND1	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	NAND_50S	NAND0	FMI0_AD<0>	6 13
	NAND_50S	NAND0	FMI0_AD<1>	6 13
	NAND_50S	NAND0	FMI0_AD<2>	6 13
	NAND_50S	NAND0	FMI0_AD<3>	6 13
	NAND_50S	NAND0	FMI0_AD<4>	6 13
	NAND_50S	NAND0	FMI0_AD<5>	6 13
	NAND_50S	NAND0	FMI0_AD<6>	6 13
	NAND_50S	NAND0	FMI0_AD<7>	6 13
	NAND_50S	NAND0	FMI0_ALE	6 13
	NAND_50S	NAND0	FMI0_CE0_L	6 13
	NAND_50S	NAND0	TP_FMI0_CE1_L	
	NAND_50S	NAND0	TP_FMI0_CE2_L	
	NAND_50S	NAND0	TP_FMI0_CE3_L	
	NAND_50S	NAND0	TP_FMI0_CE4_L	
	NAND_50S	NAND0	TP_FMI0_CE5_L	
	NAND_50S	NAND0	TP_FMI0_CE6_L	
	NAND_50S	NAND0	TP_FMI0_CE7_L	
	NAND_50S	NAND0	FMI0_CLE	6 13
	NAND_50S	NAND0	FMI0_DQS	6 13
	NAND_50S	NAND0	FMI0_RE_L	6 13
	NAND_50S	NAND0	FMI0_WE_L	6 13
	NAND_50S	NAND1	FMI1_AD<0>	6 13
	NAND_50S	NAND1	FMI1_AD<1>	6 13
	NAND_50S	NAND1	FMI1_AD<2>	6 13
	NAND_50S	NAND1	FMI1_AD<3>	6 13
	NAND_50S	NAND1	FMI1_AD<4>	6 13
	NAND_50S	NAND1	FMI1_AD<5>	6 13
	NAND_50S	NAND1	FMI1_AD<6>	6 13
	NAND_50S	NAND1	FMI1_AD<7>	6 13
	NAND_50S	NAND1	FMI1_ALE	6 13
	NAND_50S	NAND1	FMI1_CE0_L	6 13
	NAND_50S	NAND1	TP_FMI1_CE2_L	
	NAND_50S	NAND1	TP_FMI1_CE4_L	
	NAND_50S	NAND1	TP_FMI1_CE5_L	
	NAND_50S	NAND1	TP_FMI1_CE6_L	
	NAND_50S	NAND1	TP_FMI1_CE7_L	
	NAND_50S	NAND1	FMI1_CLE	6 13
	NAND_50S	NAND1	FMI1_DQS	6 13
	NAND_50S	NAND1	FMI1_RE_L	6 13
	NAND_50S	NAND1	FMI1_WE_L	6 13

WIFI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	WIFI_50S
WIFI_PWR100	*	WIFI_PWR100
WIFI_PWR1000	*	WIFI_PWR1000

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	WIFI_50S		50_WLAN_G	27
	WIFI_50S		50_WLAN_A	27
	WIFI_50S		50_WLAN_G_1	27
	WIFI_50S		50_WLAN_A_DIPLX	27
	WIFI_50S		50_WIFI_ANT_FD_2	
	WIFI_50S		50_WIFI_ANT_FD_1	
	WIFI_50S		50_WIFI_ANT_FD	

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		PWR	PPVREF_DDR0_CA	11 39
		PWR	PPVREF_DDR0_DQ	11 39
		PWR	PPVREF_DDR1_CA	11 39
		PWR	PPVREF_DDR1_DQ	11 39
		PWR	PPVREF_DDR2_CA	12 39
		PWR	PPVREF_DDR2_DQ	12 39
		PWR	PPVREF_DDR3_CA	12 39
		PWR	PPVREF_DDR3_DQ	12 39

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PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PP_PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

	VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B11	1.1V	PP_PWR	PWR	BUCK0A_LX0	29
B10	1.1V	PP_PWR	PWR	BUCK0A_LX1	29
B9	1.1V	PP_PWR	PWR	BUCK0A_FB	29
B8	1.1V	PP_PWR	PWR	PP1V1_CPU0_FET	29 30
B7	1.1V	PP_PWR	PWR	BUCK0B_LX0	29
B6	1.1V	PP_PWR	PWR	BUCK0B_LX1	29
B5	1.1V	PP_PWR	PWR	BUCK0B_FB	29
B4	1.1V	PP_PWR	PWR	PP1V1_CPU1_FET	29 30
B3	1.1V	PP_PWR	PWR	BUCK0C_LX0	29
B2	1.1V	PP_PWR	PWR	BUCK0C_FB	29
B1	1.1V	PP_PWR	PWR	PP1V1_CPUB	29 34
D13	1.2V	PP_PWR	PWR	BUCK2_LX0	29
D12	1.2V	PP_PWR	PWR	BUCK2_LX1	29
D11	1.2V	PP_PWR	PWR	BUCK2_LX2	29
D10	1.2V	PP_PWR	PWR	BUCK2_FB	29
D14	1.2V	PP_PWR	PWR	PP1V2_SOC	29 34
D16	1.8V	PP_PWR	PWR	BUCK3_LX0	29
D15	1.8V	PP_PWR	PWR	BUCK3_FB	29
D17	1.8V	PP_PWR	PWR	PP1V8_S2R	29 34
D18	1.2V	PP_PWR	PWR	BUCK4_LX0	29
D19	1.2V	PP_PWR	PWR	BUCK4_FB	29
D20	1.2V	PP_PWR	PWR	PP1V2_S2R	29 34
D21	1.1V	PP_PWR	PWR	BUCK5_LX0	29
D22	1.1V	PP_PWR	PWR	BUCK5_FB	29
D23	3.3V	PP_PWR	PWR	PP3V3_OUT	29 34
D24	3.0V	PP_PWR	PWR	PP3V0_GRAPE	29 34
D25	1.7V	PP_PWR	PWR	PP1V7_VA_VCP	19 29 34
D26	3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
D27	3.2V	PP_PWR	PWR	LDO5	29
D28	3.3V	PP_PWR	PWR	PP3V3_ACC	29 34
D29	3.0V	PP_PWR	PWR	PP3V0_S2R_HALL	29 34
D30	3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
D31	3.0V	PP_PWR	PWR	PP3V0_IO	29 34
D32	3.0V	PP_PWR	PWR	PP3V0_SENSOR	29 34
D33	2.8V	PP_PWR	PWR	PP2V8_CAM	29 34
D34	1.0V	PP_PWR	PWR	PP1V0	29 34
D35	1.1V	PP_PWR	PWR	PP1V1_SRAM	29 34
D36	1.8V	PP_PWR	PWR	PP1V8_ALWAYS	29 34
D37	1.2V	PP_PWR	PWR	PP1V2	29 34
D38		PP_PWR	PWR	DSP_SW	
D39	1.8V	PP_PWR	PWR	PP1V8	29 32 34
D40	1.8V	PP_PWR	PWR	PP1V8_GRAPE	
D41	4.7V	PP_PWR	PWR	PPVCC_MAIN	15 25 29 30 34
D42	4.2V	PWR500	PWR	PPBATT_VCC	29 32 34
D43	6.0V	PP_PWR	PWR	PP6V0_LCM_HI	30
D44	6.0V	PP_PWR	PWR	LCM_LX	30
D45	6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST	30
D46	5.25V	PP_PWR	PWR	PP5V25_VLCM1	
D47	1.1V	PP_PWR	PWR	PP1V1_CPU0	30 34
D48	1.1V	PP_PWR	PWR	PP1V1_CPU1	30 34
D49	20.4V	PP_PWR	PWR	PPLED_OUT_A	30 34
D50	20.4V	PP_PWR	PWR	PPLED_OUT_B	30 34
D51	1.8V	PP_PWR	PWR	PP1V8_PL0_F	4
D52	1.0V	PP_PWR	PWR	PP1V0_MIPI_PLL_F	7
D53	1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX	7
D54	1.8V	PP_PWR	PWR	PP1V8_DP_AVDD_AUX	
D55	3.3V	PP_PWR	PWR	PP3V3_S0_LCD_FERR	15
D56	3.3V	PP_PWR	PWR	PP3V3_LCDVDD_SW_F	15
D57	20.4V	PWR500	PWR	PPLED_BACK_REG_B	15
D58	20.4V	PP_PWR	PWR	PPLED_BACK_REG_A	15
D59	6V	PP_PWR	PWR	PPVBUS_USB_EMI	23 34
D60	0.6V	PP_PWR	PWR	PPVREF_DDR0_CA	11 38
D61	0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ	11 38
D62	0.6V	PP_PWR	PWR	PPVREF_DDR1_CA	11 38
D63	0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ	11 38
D64	0.6V	PP_PWR	PWR	PPVREF_DDR2_CA	12 38
D65	0.6V	PP_PWR	PWR	PPVREF_DDR2_DQ	12 38
D66	0.6V	PP_PWR	PWR	PPVREF_DDR3_CA	12 38
D67	0.6V	PP_PWR	PWR	PPVREF_DDR3_DQ	12 38
D68		PP_PWR	PWR	DAC_AP_VREF	7
D69	4.6V	PP_PWR	PWR	BATT_POS_RC	29
D70	4.6V	PP_PWR	PWR	BATT_VCC_WLAN	27
D71	1.8V	PP_PWR	PWR	PP_WLAN_VDDIO_1V8	27
D72	3.55V	PP_PWR	PWR	LDO10	18 29

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_PH

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B10	VOLTAGE=0V	GND	GND	GND	
B12	VOLTAGE=0V	GND	GND	GND_AUDIO_CODEC	18
B11	VOLTAGE=0V	GND	GND	GND_SPKR_AMP1	
B13	VOLTAGE=0V	GND	GND	GND_SPKR_AMP2	
B15	VOLTAGE=0V	GND	GND	AGND_U3000	16
B22	VOLTAGE=0V	GND	GND	J2200_29_GND	15
B23	VOLTAGE=0V	GND	GND	J2200_36_GND	15
B24	VOLTAGE=0V	GND	GND	J2200_43_GND	15

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
B16			RST	BB_TRST_L	
B17			RST	DBG_RST	
B18			RST	DEBUG_RST_L	
B19			RST	GSM_TXBURST_IND	
B20			RST	JTAG_AP_TRST_L	4 10 36
B21			RST	RST_AP_1V8_L	
B22			RST	RST_AP_L	4 25 26 30
B23			RST	GPIO_BB_RST_L	5 26
B24			RST	RST_BB_PMU_L	
B25			RST	RST_BT_L	
B26			RST	RST_DET_L	
B27			GRAPE	RST_GRAPE_L	
B28			RST	RST_L63_L	
B29			RST	RST_PMU_IN	
B30			RST	RST_WLAN_L	
B31			RST	SIMCRD_RST	
B32			RST	UD881_RST	
B33			RST	UD882_RST	

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