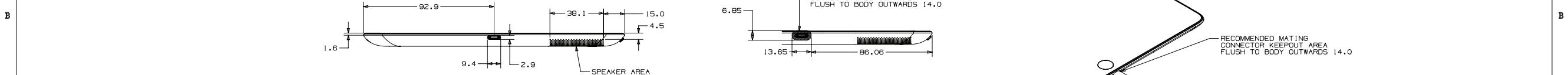
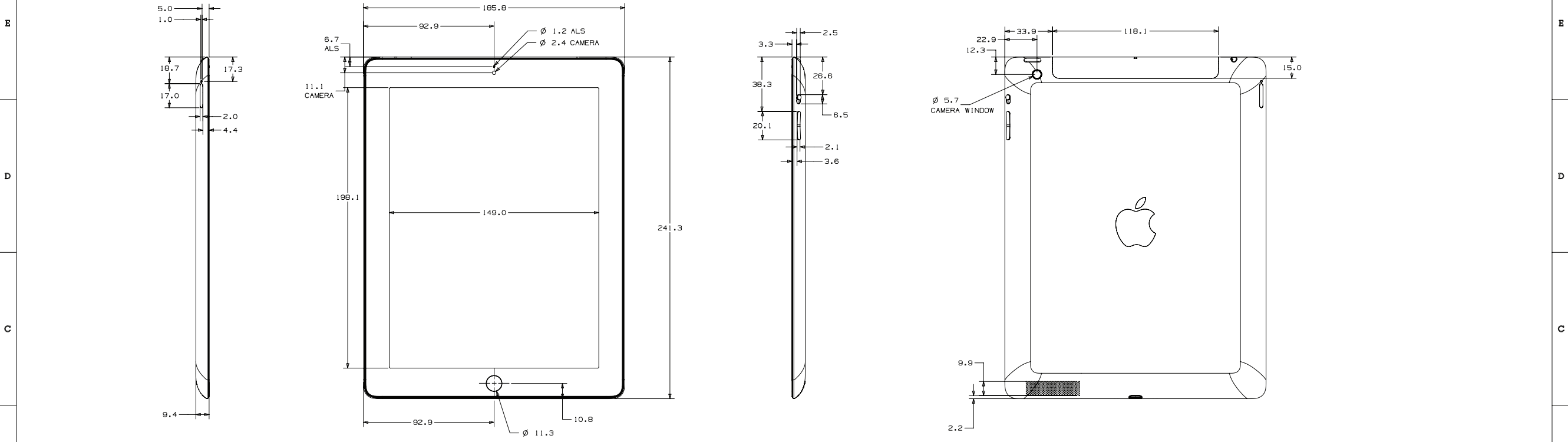
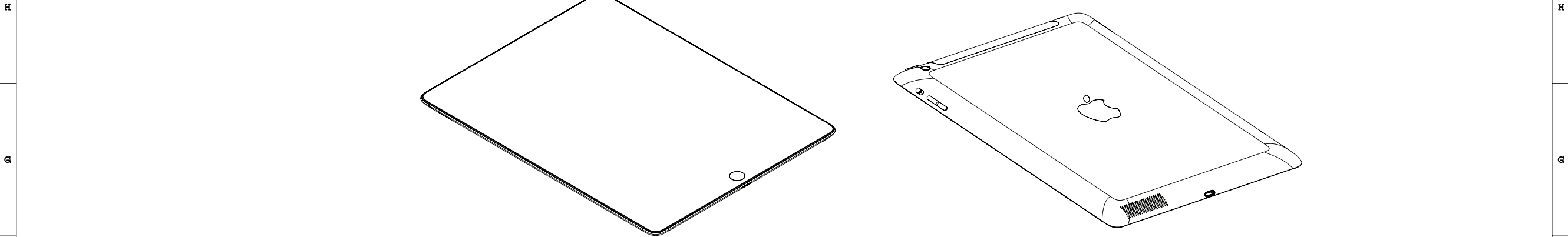


NOTES (UNLESS OTHERWISE SPECIFIED)



www.vinafix.vn

87654321

REV: E004

DESCRIPTION OF REVISION

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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

iPad 4th Gen

LAST\_MODIFIED=Thu Jul 26 10:29:36 2012

REV

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ECN

0001554595

DESCRIPTION OF REVISION

PRODUCTION RELEASED

CK APPD

DATE

2012-07-26

PDF CSA CONTENTS

1123456789101112131415161718192021222324252627282930

Table of Contents

BLOCK DIAGRAM: SYSTEM

BOM TABLES

AP: MAIN

AP: I/Os

AP: NAND

AP: TV,DP,MIPI

AP: DDR

AP: POWER

AP: MISC & ALIASES

DDR 0 AND 1

DDR 2 AND 3

NAND

ALIASES

VIDEO: EDP CONNECTOR

GRAPE: GROUNDHOG,CONN,BOOST

GRAPE: Z1, Z2

AUDIO: L81 CODEC

AUDIO: SPEAKER AMP

SENSOR FLEX CONN

SENSOR CONN FILTERS 1

SENSOR CONN FILTERS 2

E75 DOCK SUPPORT

IO FLEX CONN

TRISTAR

CONNECTOR: CELLULAR

WIFI/BT

POWER: BATTERY CONNECTOR

PMU: ADRIANA PAGE 1

PMU: ADRIANA PAGE 2

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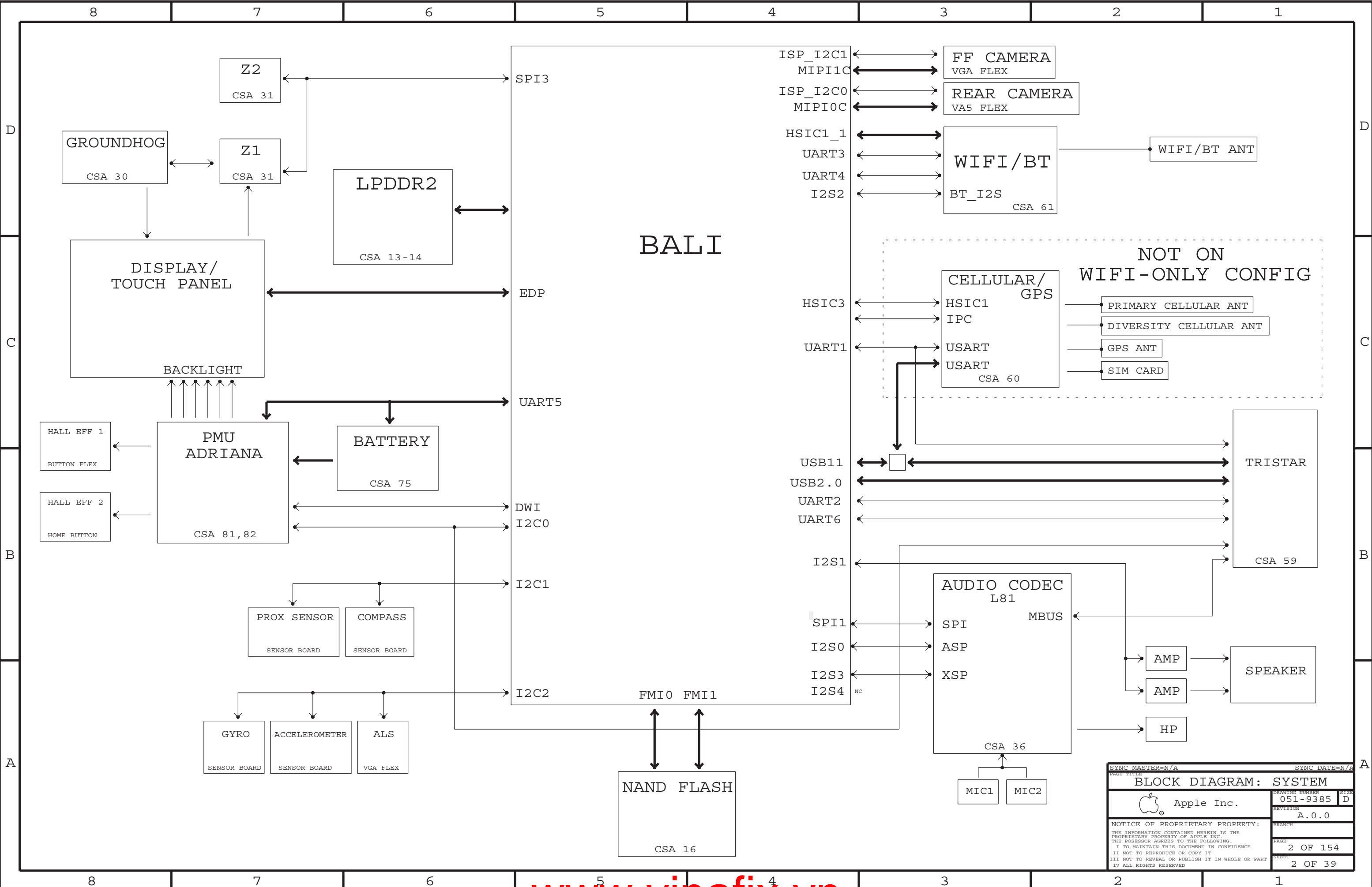
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Power aliases required by this page:  
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Signal aliases required by this page:  
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BOM options provided by this page:

```
COMMON
ALTERNATE

16GB PROD: 16GB CONFIG
32GB PROD: 32GB CONFIG
64GB PROD: 64 GB CONFIG
DEV: DEV BOARD ONLY

MLB: MLB BOARD ONLY
MLB A: WIFI ONLY CONFIG
MLB B: CELLULAR CONFIG
MLB C: CELLULAR CONFIG
MLB D: LEGACY CELLULAR CONFIG
MLB E: LEGACY CELLULAR CONFIG
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-4195	1	FENCE,NAND,TOP,MLB,X140	PD_FENCE_NAND	CRITICAL	
806-3493	1	FENCE,LARGE,TOP,MLB,X140	PD_FENCE_LARGE	CRITICAL	
806-3956	1	FENCE,AMP,MLB,X140	PD_FENCE_AMP	CRITICAL	
806-4196	1	FENCE, 1, BTM, MLB, X140	PD_FENCE_BT1	CRITICAL	
806-3492	1	FENCE, 2, BTM, MLB, X140	PD_FENCE_BT2	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7838	1	EEEE FOR 639-3736 (MLB A 16G)	EEEE_F1WD	CRITICAL	EEEE_MLB_A_16G
825-7838	1	EEEE FOR 639-3737 (MLB A 32G)	EEEE_F1WH	CRITICAL	EEEE_MLB_A_32G
825-7838	1	EEEE FOR 639-3738 (MLB A 64G)	EEEE_F1N8	CRITICAL	EEEE_MLB_A_64G
825-7838	1	EEEE FOR 639-4176 (MLB A 128G)	EEEE_F8Q4	CRITICAL	EEEE_MLB_A_128G
825-7838	1	EEEE FOR 639-3263 (MLB B 16G)	EEEE_DWKG	CRITICAL	EEEE_MLB_B_16G
825-7838	1	EEEE FOR 639-3739 (MLB B 32G)	EEEE_F1W7	CRITICAL	EEEE_MLB_B_32G
825-7838	1	EEEE FOR 639-3740 (MLB B 64G)	EEEE_F1NC	CRITICAL	EEEE_MLB_B_64G
825-7838	1	EEEE FOR 639-4177 (MLB B 128G)	EEEE_F8P0	CRITICAL	EEEE_MLB_B_128G
825-7838	1	EEEE FOR 639-3741 (MLB C 16G)	EEEE_F1NG	CRITICAL	EEEE_MLB_C_16G
825-7838	1	EEEE FOR 639-3742 (MLB C 32G)	EEEE_F1WF	CRITICAL	EEEE_MLB_C_32G
825-7838	1	EEEE FOR 639-3743 (MLB C 64G)	EEEE_F1N9	CRITICAL	EEEE_MLB_C_64G
825-7838	1	EEEE FOR 639-4178 (MLB C 128G)	EEEE_F8OR	CRITICAL	EEEE_MLB_C_128G

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9385	1	SCH,MLB,X140	SCH1	CRITICAL	
820-3249	1	PCBF,MLB,X140	PCB1	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0598	1	IC, SOC, H5G, FCBGA1089, 0.5MM	U0600	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0622	1	IC, PMU, ADRIANA, D2018A1, FCBGA	U8100	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0636	2	LPDDR2,533MHZ,512MB,SAMSUNG,35NM	U1300,U1400	CRITICAL	

NAND					
16GB FLASH CONFIGURATIONS					
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0878	1	TOSHIBA PPN1.5 16GB	U1600	CRITICAL	16GB_PROD


## 16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM_OPTION
335S0878	1	TOSHIBA PPN1.5 16GB	U1600	CRITICAL	16GB_PROD

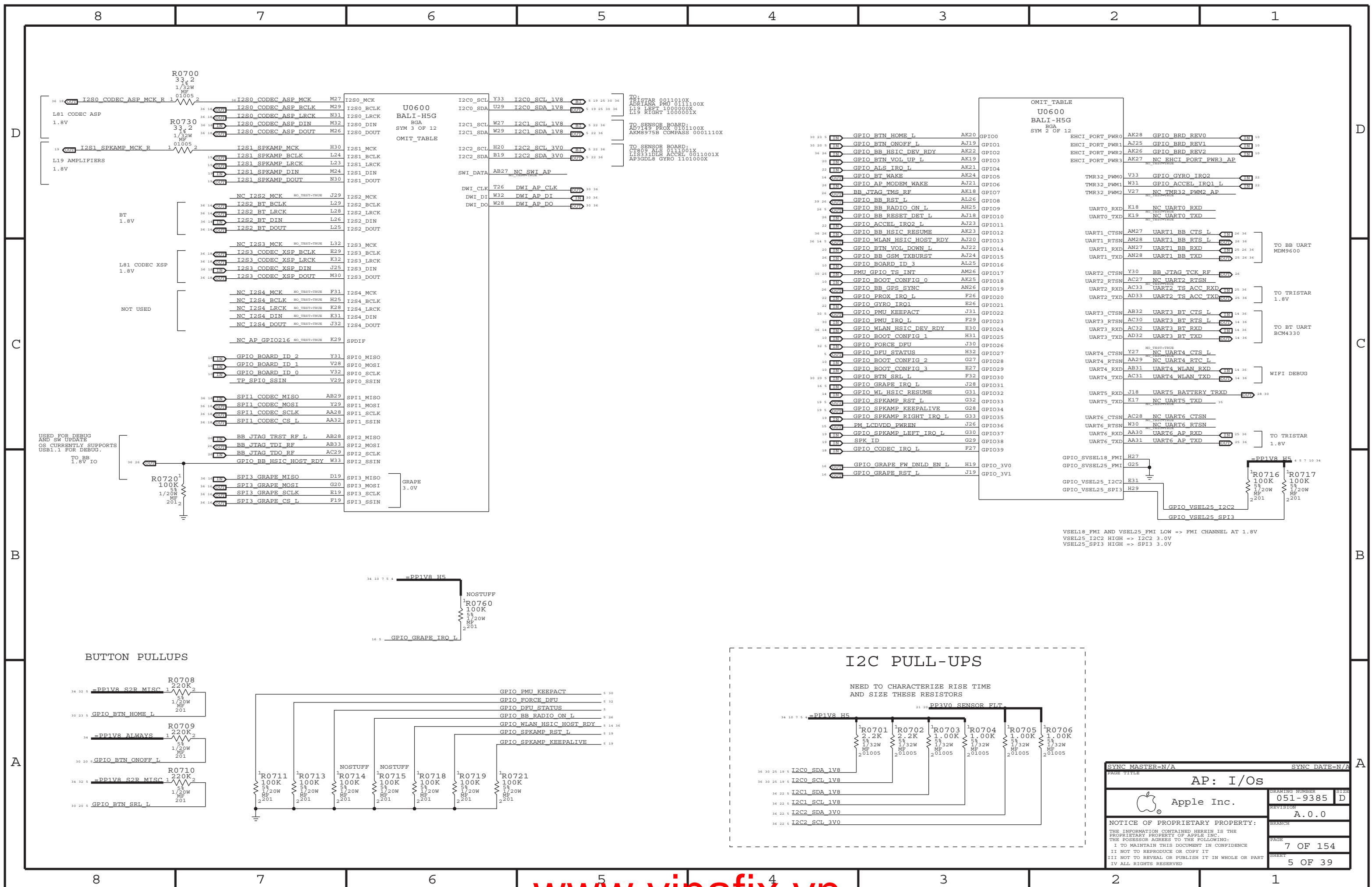
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335S0879	1	TOSHIBA PPN1.5 32GB	U1600	CRITICAL	32GB__PROD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM_OPTION
335S0880	1	TOSHIBA PPN1.5 64GB	U1600	CRITICAL	64GB_PROD

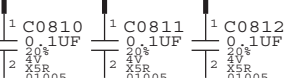
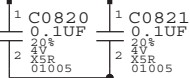
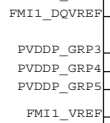
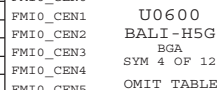
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335S0912	1	TOSHIBA PPN1.5 128GB	U1600	CRITICAL	128GB_PROD

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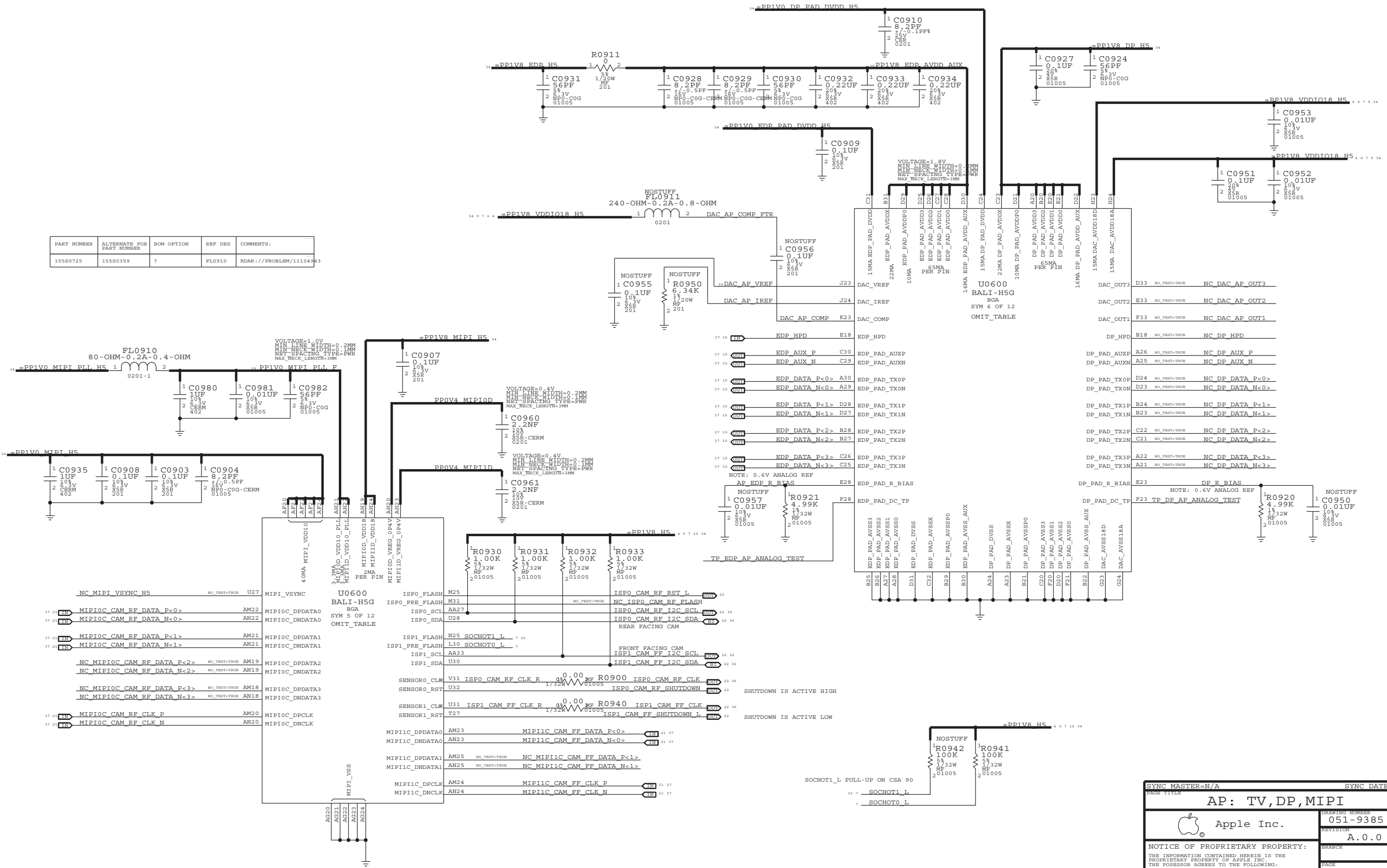
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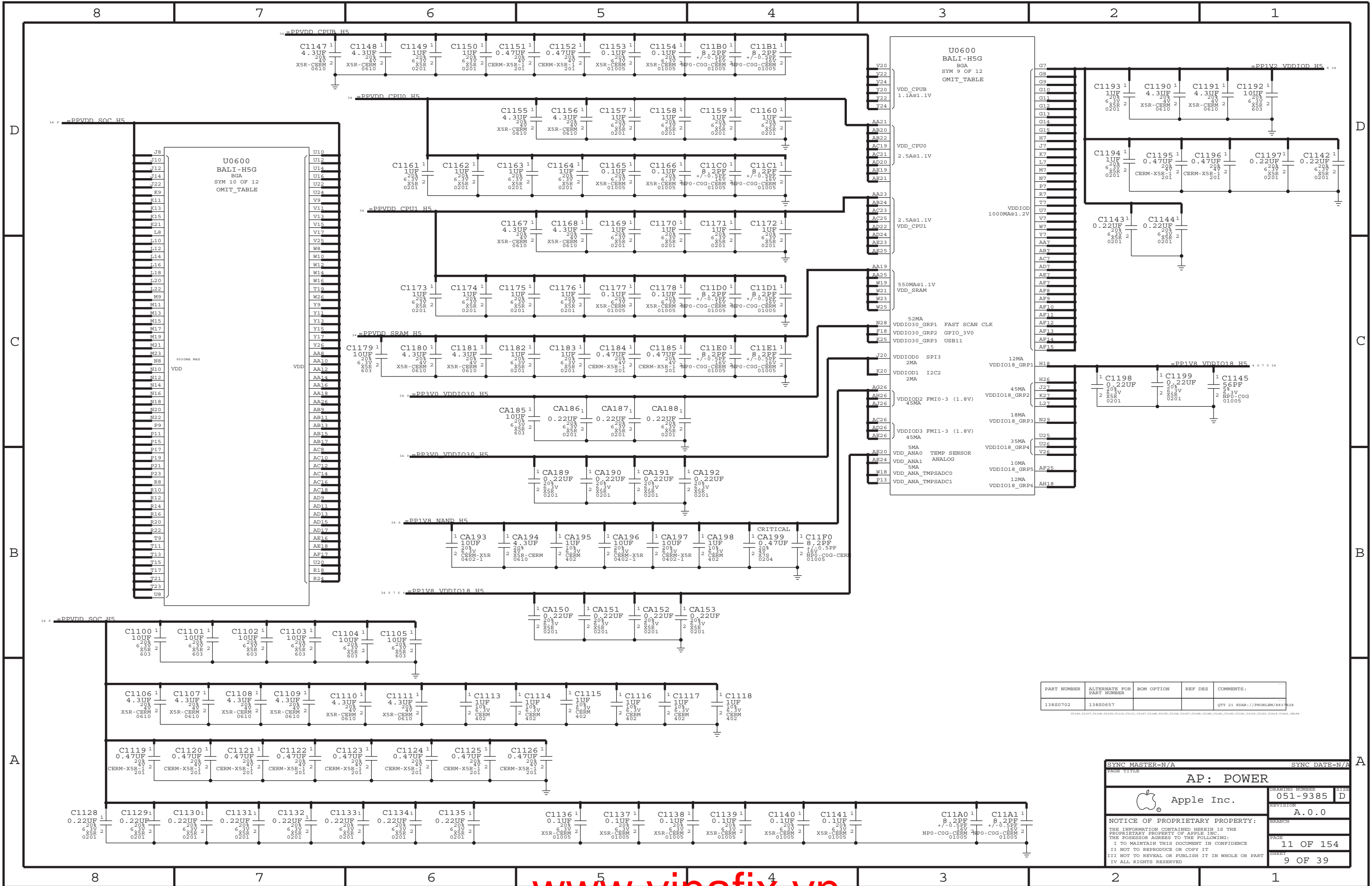
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657			QTY 21 RDR: // PROBLEM/83728

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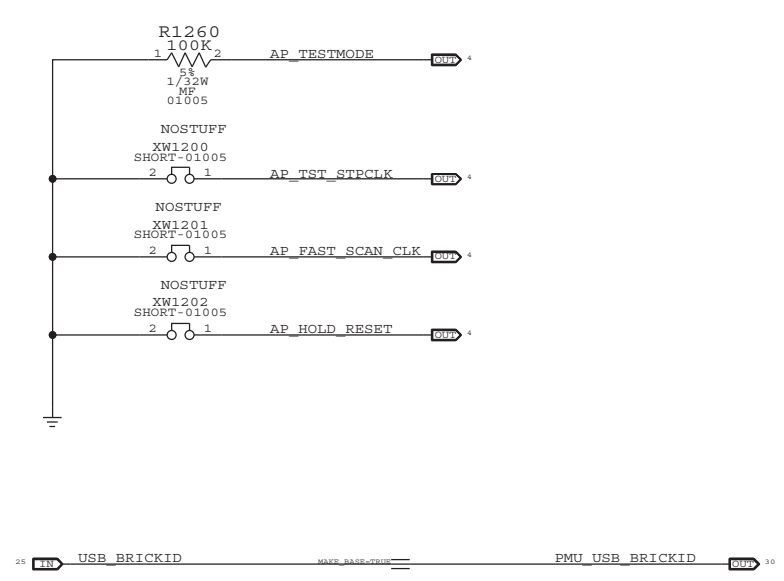
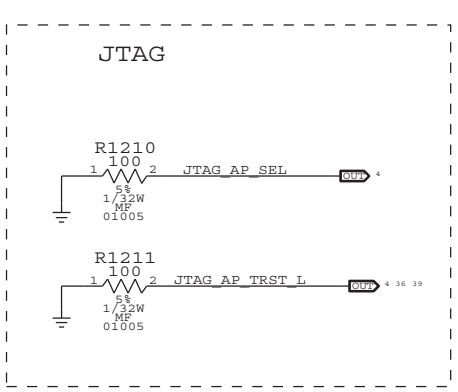
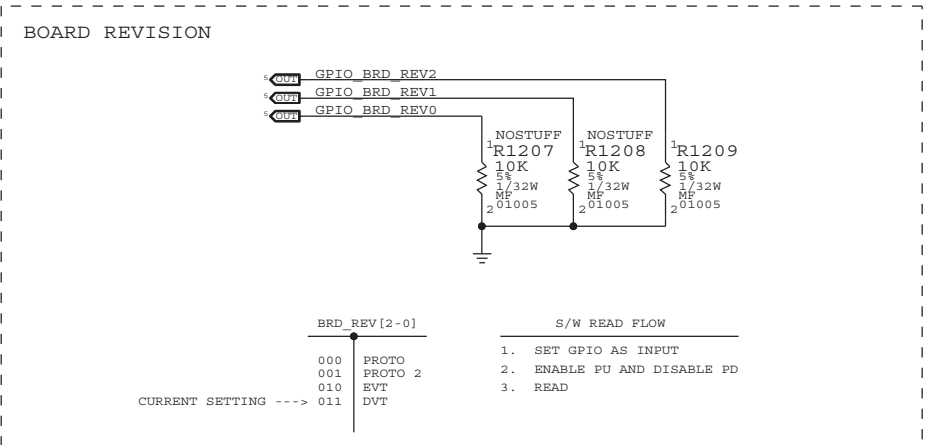
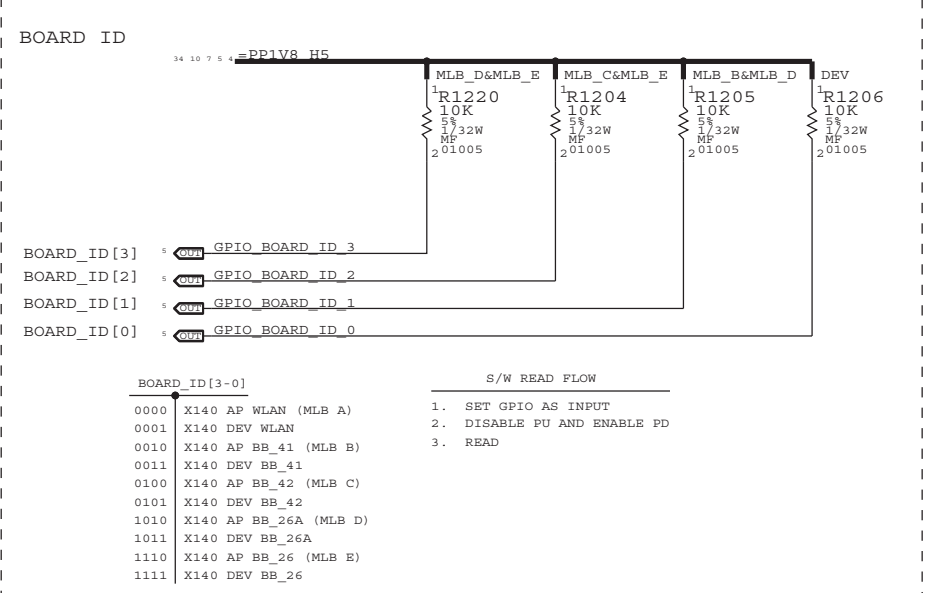
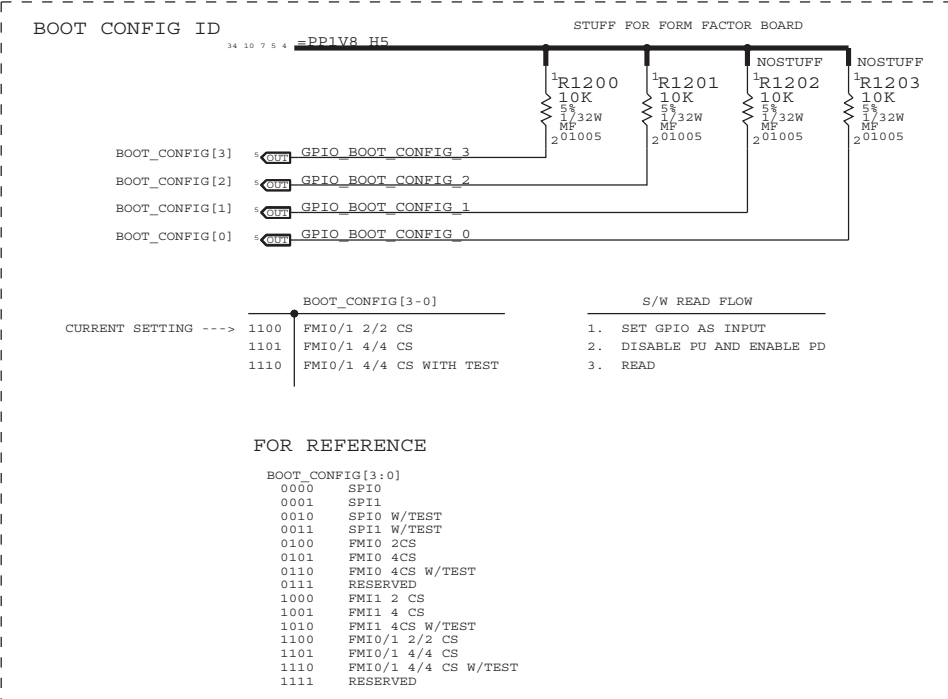
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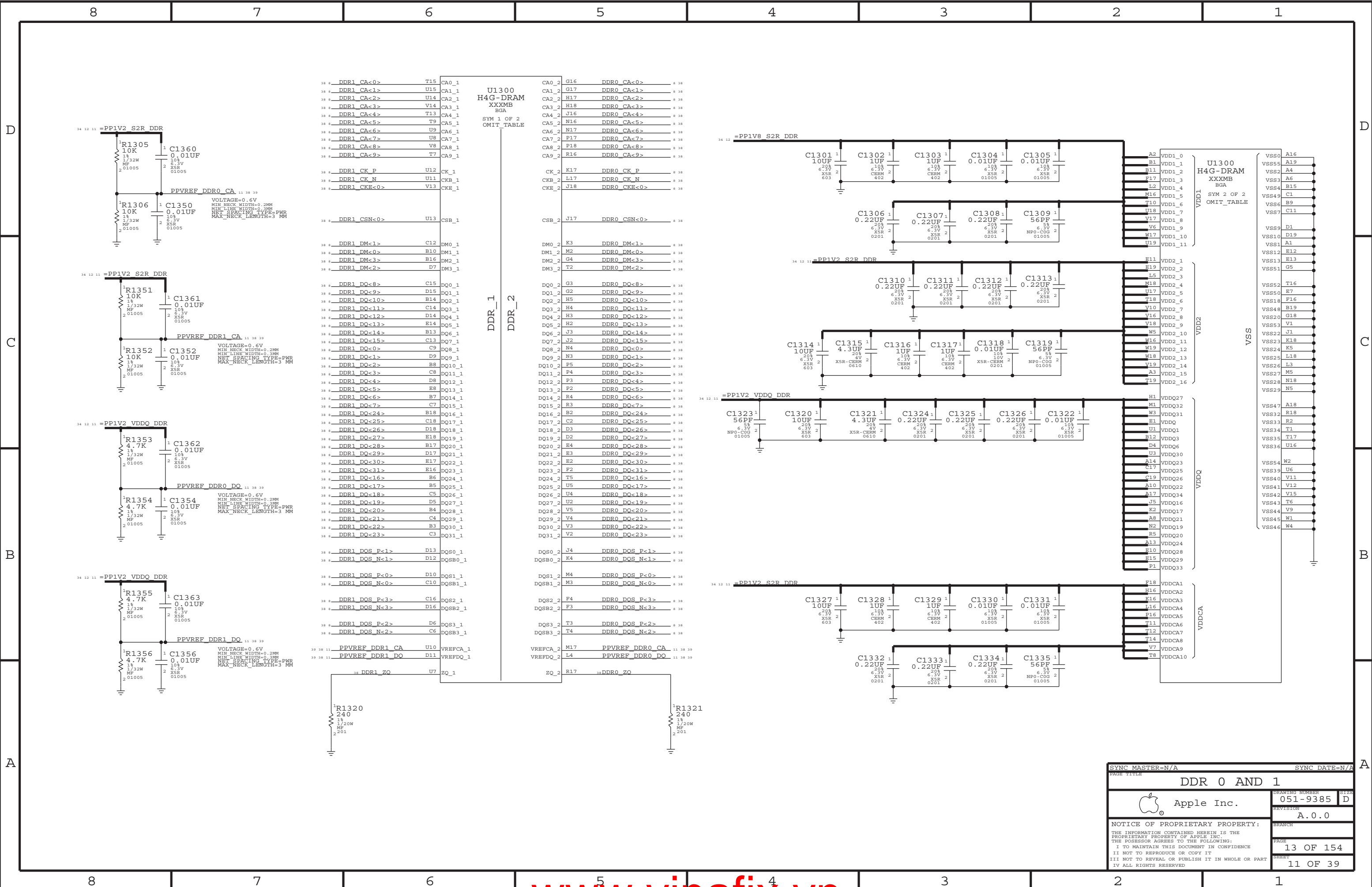
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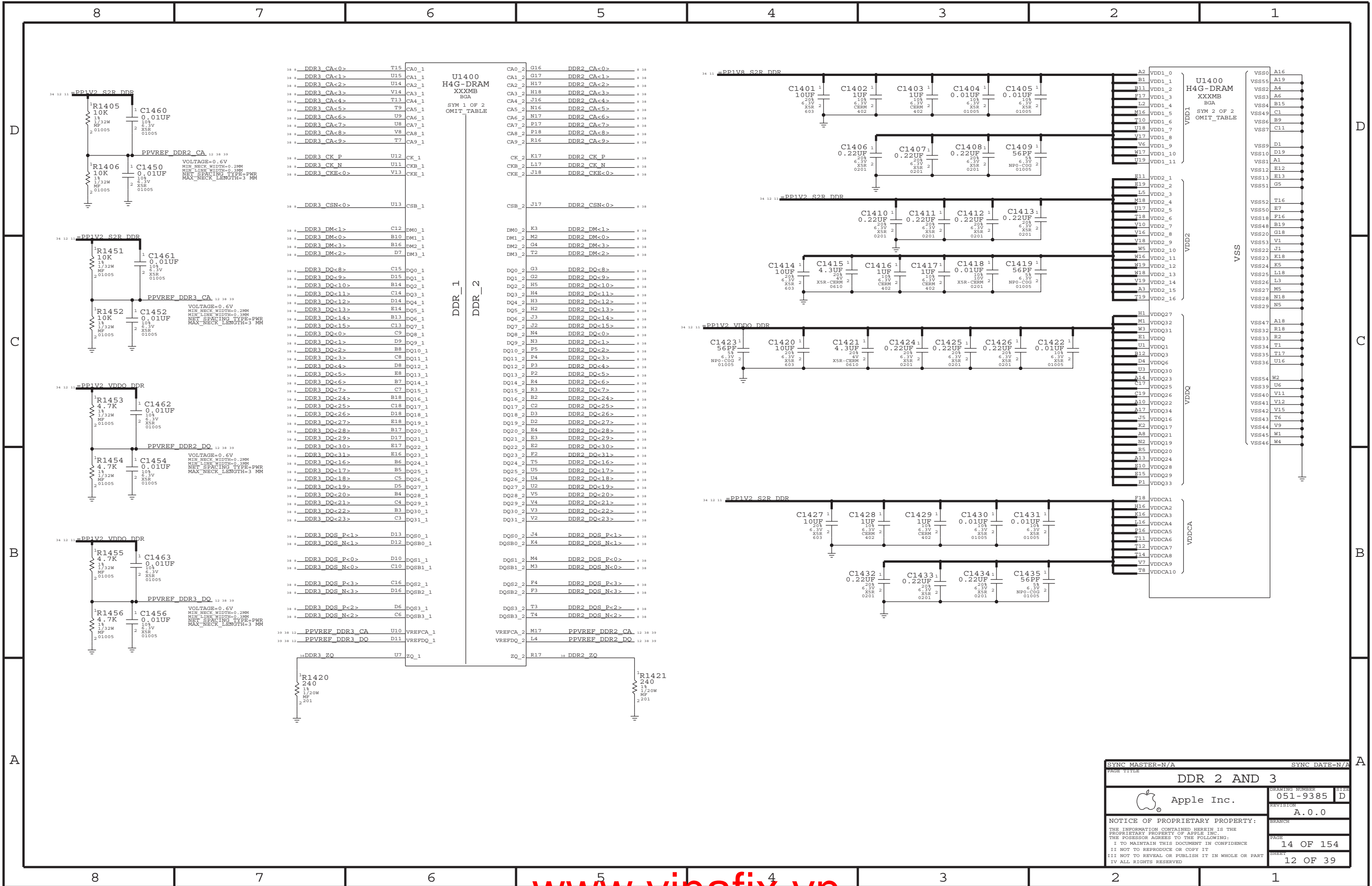


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XXXMB  
BGA

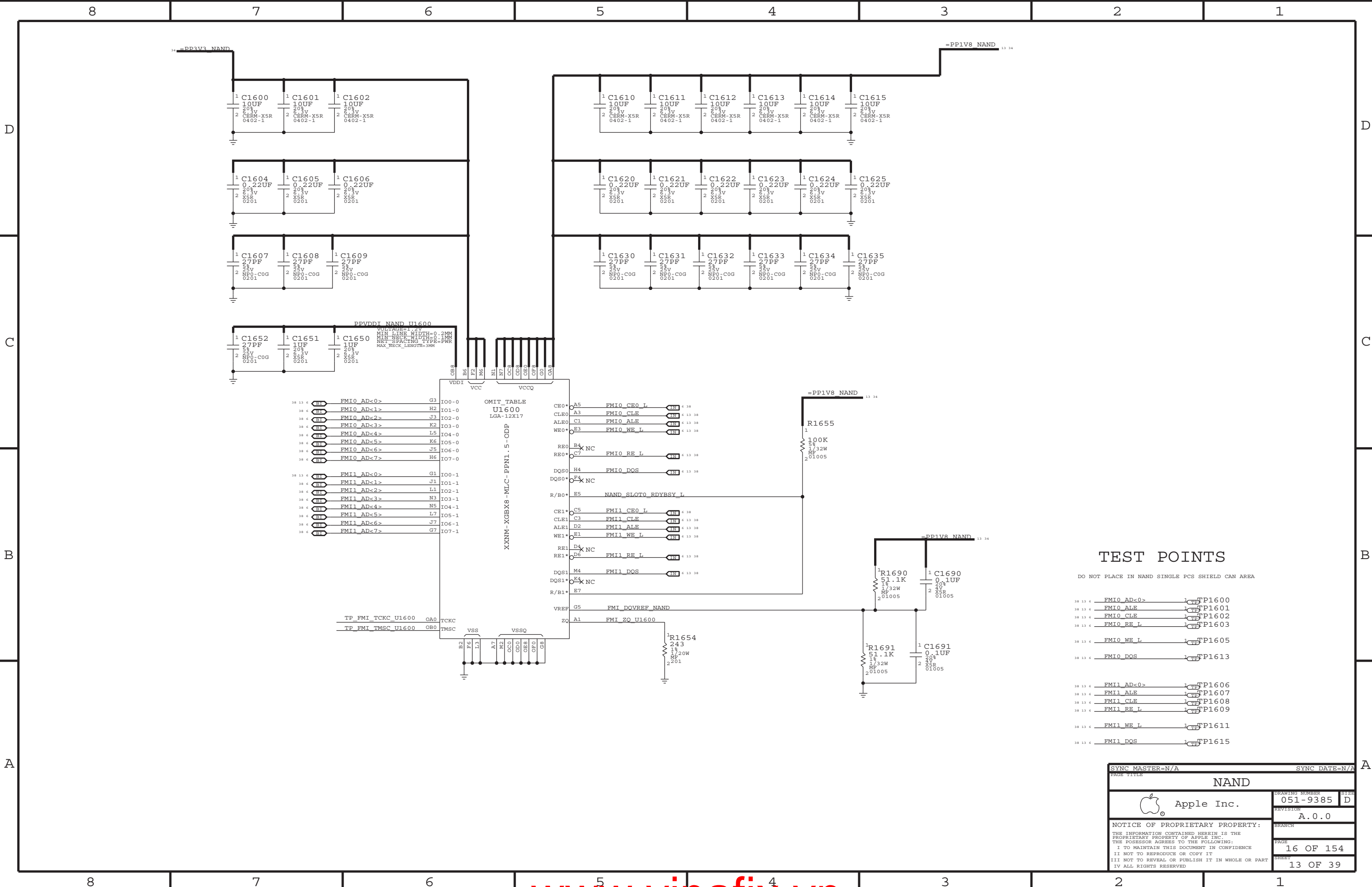
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DDR\_2

U1300  
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XXXMB  
BGA

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WIFI ALIASES

36	4	HSIC1 WLAN_DATA	MAKE_BROG-TMUS	50	HSIC WLAN_DATA	27
36	4	HSIC1 WLAN_STB	MAKE_BROG-TMUS	50	HSIC WLAN STROBE	27
36	5	GPIO WLAN_HSIC_HOST_RDY	MAKE_BROG-TMUS	AP	HSIC3_RDY	27
36	5	GPIO WLAN_HSIC_DEV_RDY	MAKE_BROG-TMUS	DEV	HSIC3_RDY	27
30		PMU_GPIO WLAN_REG_ON	MAKE_BROG-TMUS	WLAN	REG_ON	27
30		PMU_GPIO WLAN_HOST_WAKE	MAKE_BROG-TMUS	HOST	WAKE WLAN	27
30		PMU_GPIO_BT_REG_ON	MAKE_BROG-TMUS	BT	REG_ON	27
30		PMU_GPIO_BT_HOST_WAKE	MAKE_BROG-TMUS	HOST	WAKE_BT	27
5		GPIO_BT_WAKE	MAKE_BROG-TMUS	BT	WAKE	27
36	5	UART3_BT_RXD	MAKE_BROG-TMUS	BT	UART_TXD	27
36	5	UART3_BT_TXD	MAKE_BROG-TMUS	BT	UART_RXD	27
36	5	UART3_BT_CTS_L	MAKE_BROG-TMUS	BT	UART_RTS_L	27
36	5	UART3_BT_RTS_L	MAKE_BROG-TMUS	BT	UART_CTS_L	27
36	30	PMU_GPIO_CLK_32K_WLAN	MAKE_BROG-TMUS	CLK32K	AP	27
36	5	I2S2_BT_BCLK	MAKE_BROG-TMUS	BT	PCM_CLK	27
36	5	I2S2_BT_DOUT	MAKE_BROG-TMUS	BT	PCM_IN	27
36	5	I2S2_BT_DIN	MAKE_BROG-TMUS	BT	PCM_OUT	27
36	5	I2S2_BT_LRCK	MAKE_BROG-TMUS	BT	PCM_SYNC	27
36	5	UART4_WLAN_RXD	MAKE_BROG-TMUS	WLAN	UART_TXD	27
36	5	UART4_WLAN_TXD	MAKE_BROG-TMUS	WLAN	UART_RXD	27
5		GPIO_WL_HSIC_RESUME	MAKE_BROG-TMUS	WLAN	HSIC3_RESUME	27
34		VDDIO_WLAN_BT_1V8	MAKE_BROG-TMUS	PP_WL_BT	VDDIO_AP	27

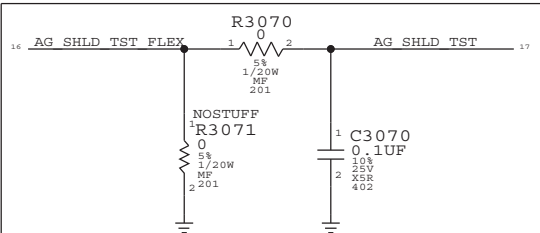
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RADAR: //PROBLEM/9015335

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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## CONNECTORS TO GRAPE FLEX



P/N 518S0828

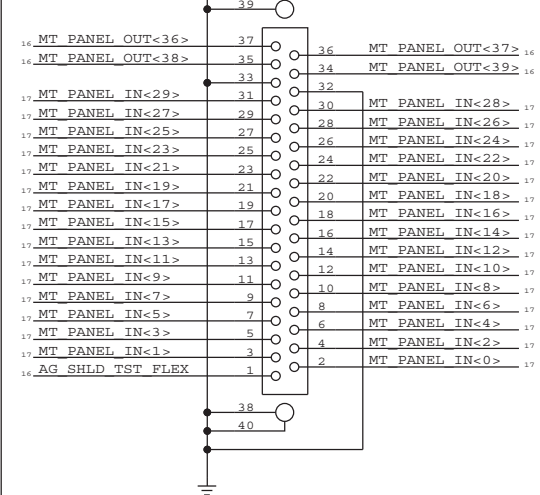
MATES WITH LEFTMOST GRAPE FLEX TAIL

CRITICAL

J3010

502250-8037-B

F-RT-SM



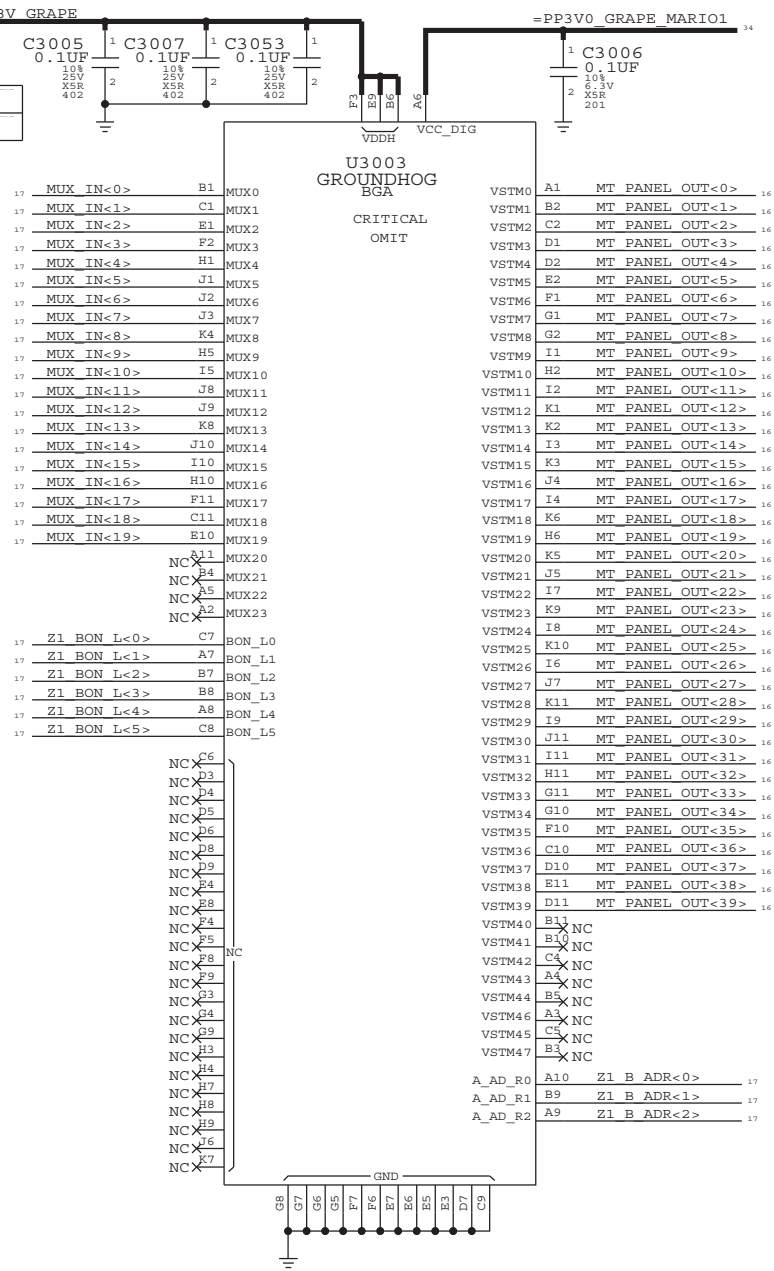
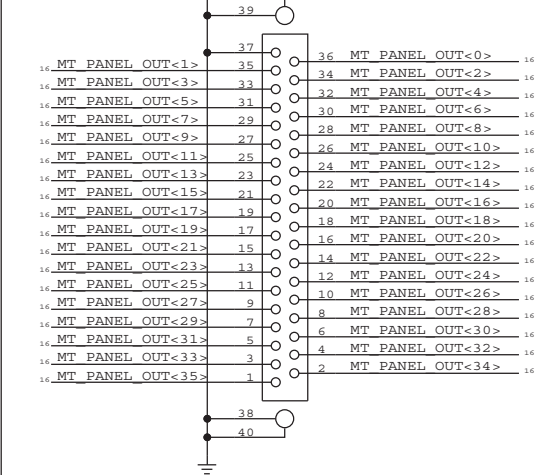
MATES WITH RIGHTMOST GRAPE FLEX TAIL

CRITICAL

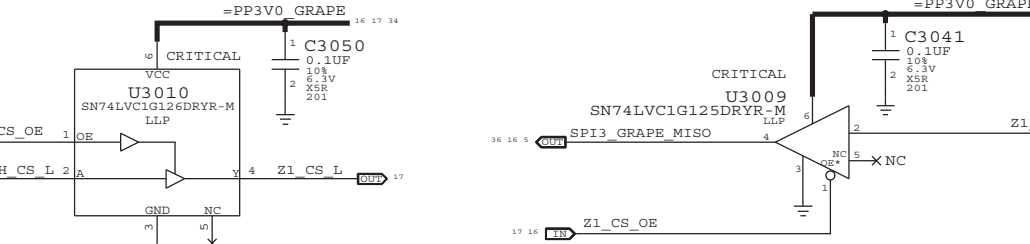
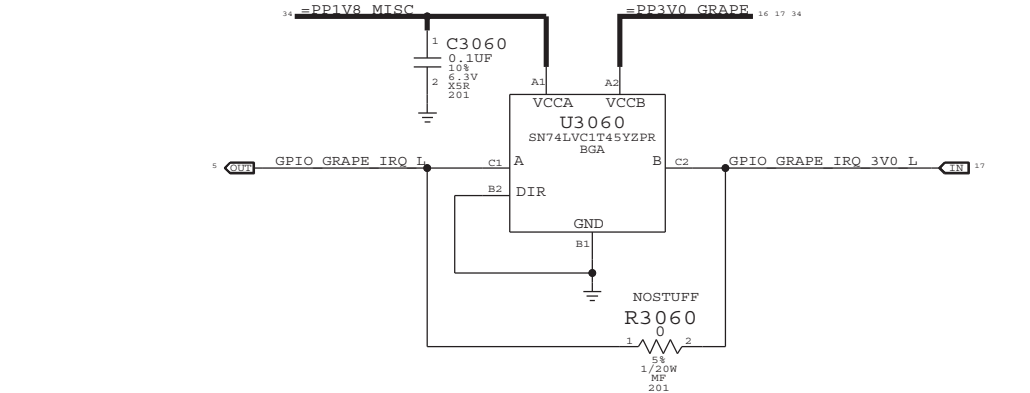
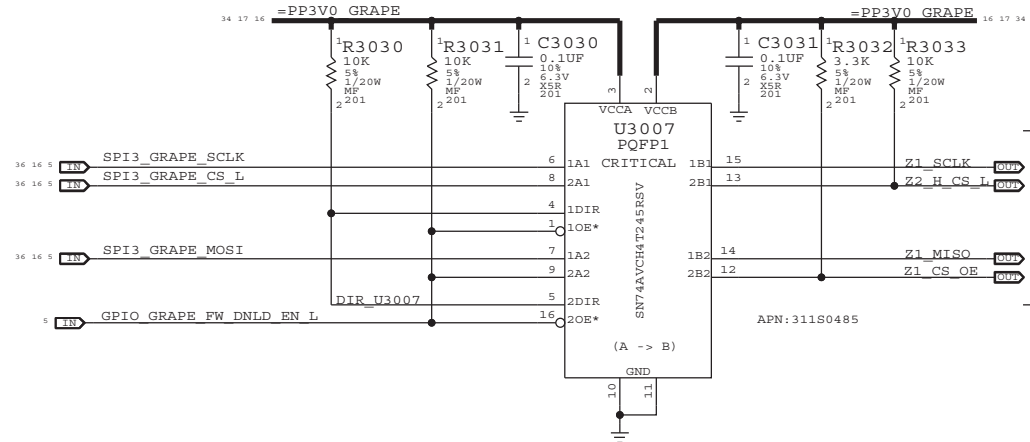
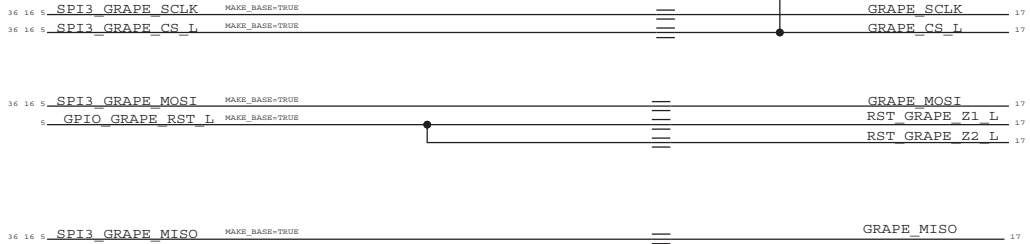
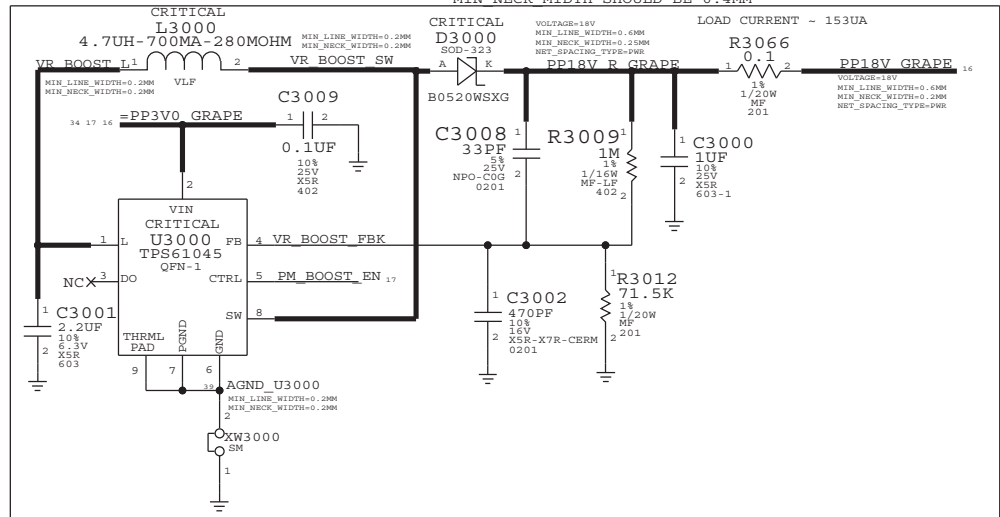
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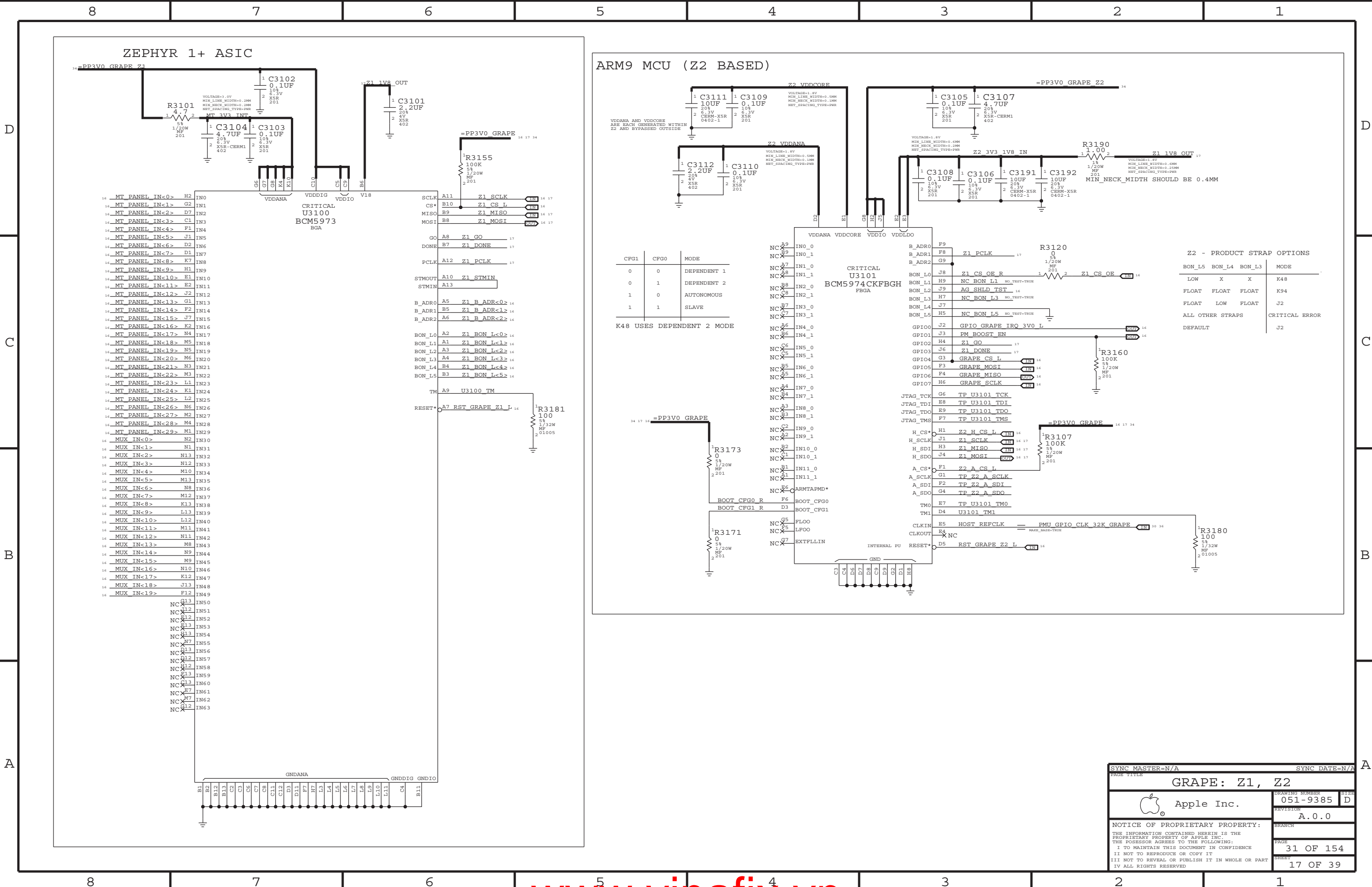


## BOOST CONVERTOR



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311S0525	311S0532		U3010	

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GRAPE: GROUNDHOG, CONN, BOOST		051-9385	
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### ARM9 MCU (Z2 BASED)

CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

K48 USES DEPENDENT 2 MODE

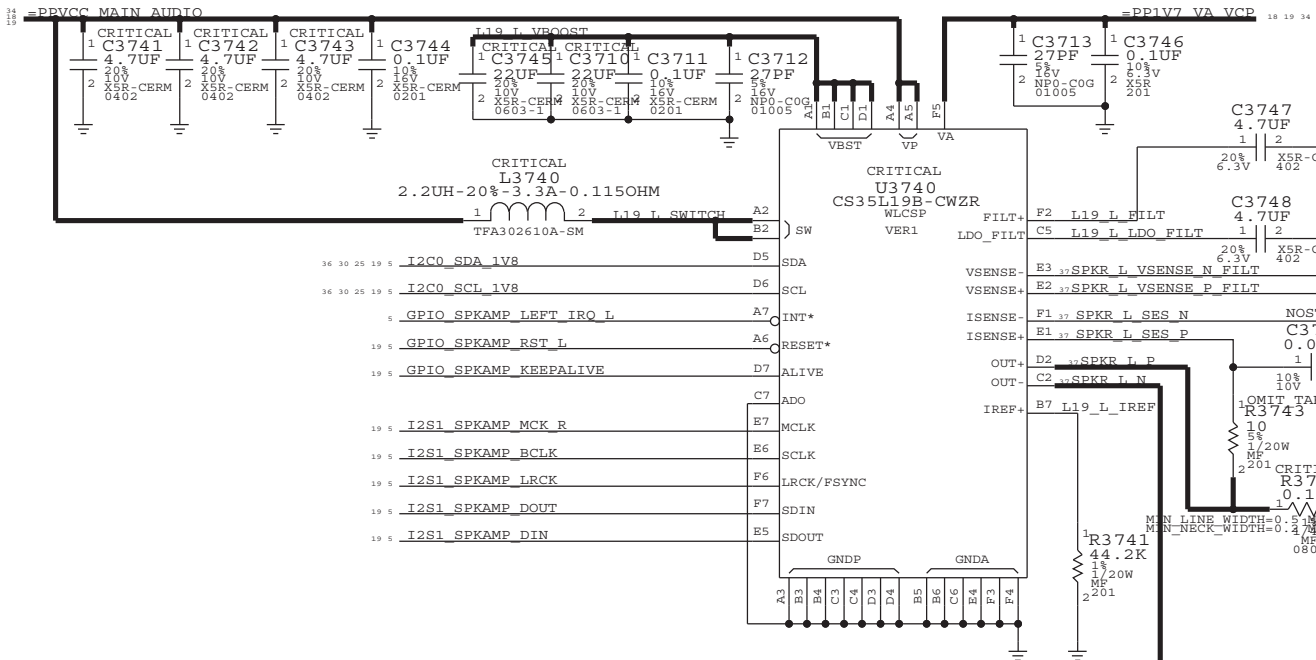
Z2 - PRODUCT STRAP OPTIONS			
BON_L5	BON_L4	BON_L3	MODE
LOW	X	X	K48
FLOAT	FLOAT	FLOAT	K94
FLOAT	LOW	FLOAT	J2
ALL OTHER STRAPS			CRITICAL ERROR
DEFAULT			J2





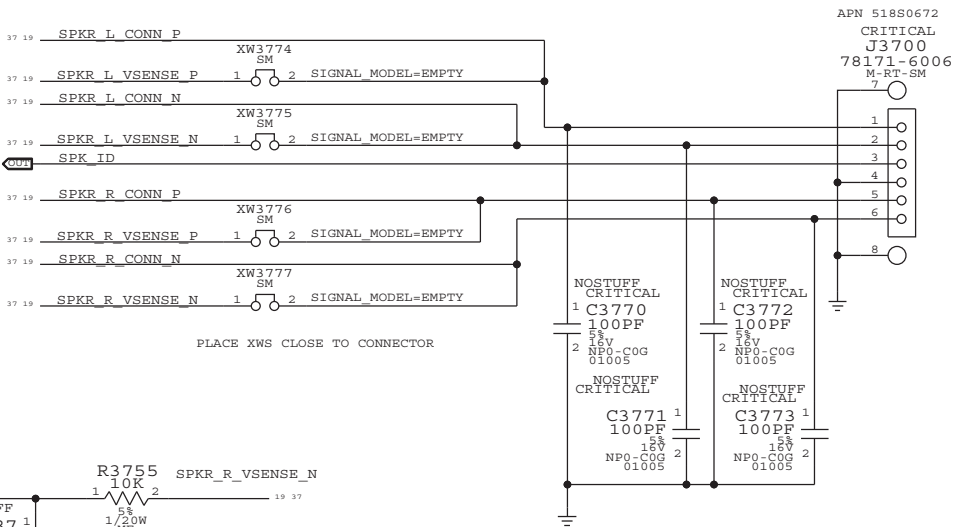
LEFT SPEAKER AMP

I2C ADDRESS: 1000000X



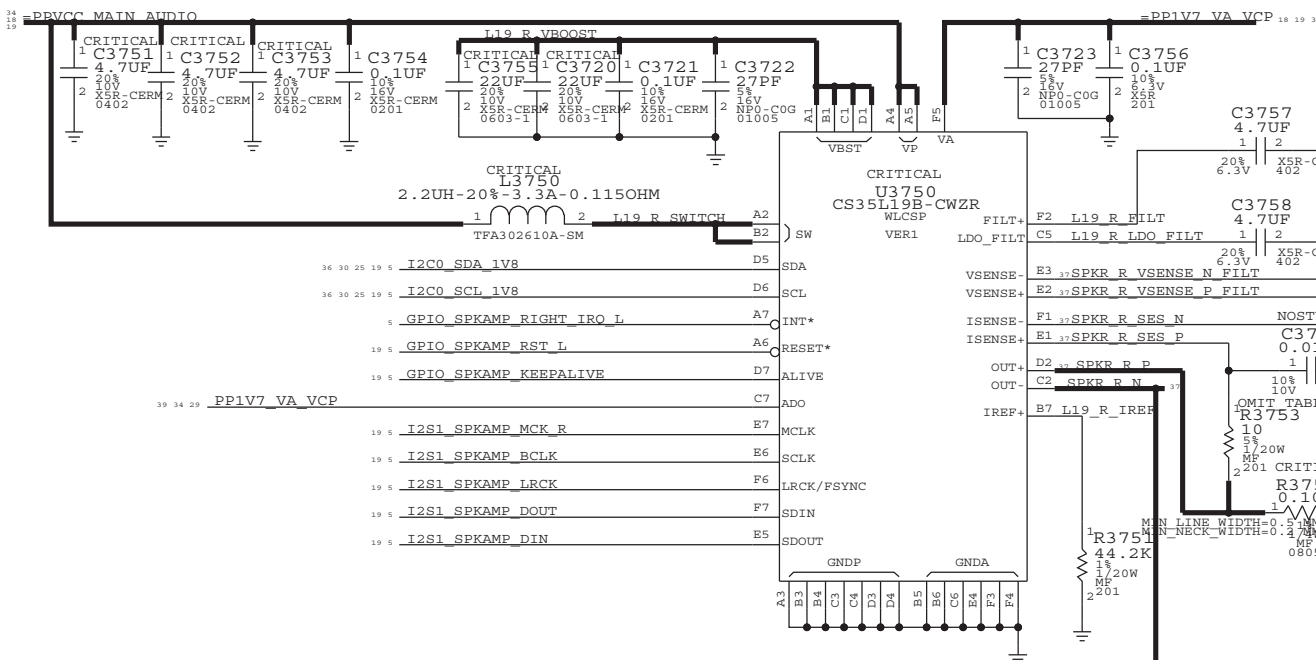
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113S0022	4	RES,MP,1/10W,00HM,5,0603,SMD,LF	FL3740,FL3741,FL3750,FL3751	?	?

SPEAKER CONNECTOR



RIGHT SPEAKER AMP

I2C ADDRESS: 1000001X



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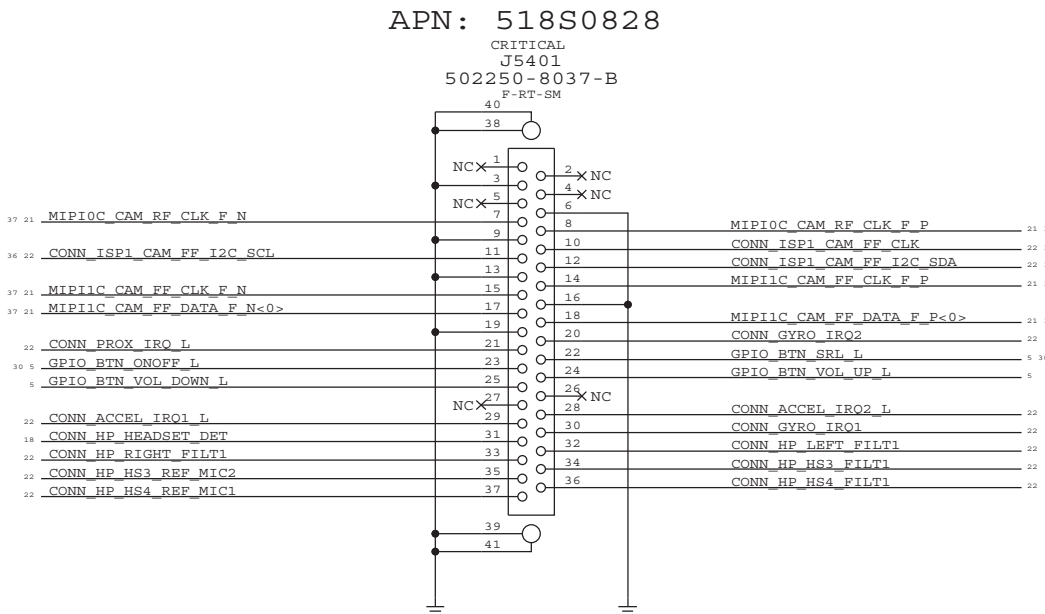
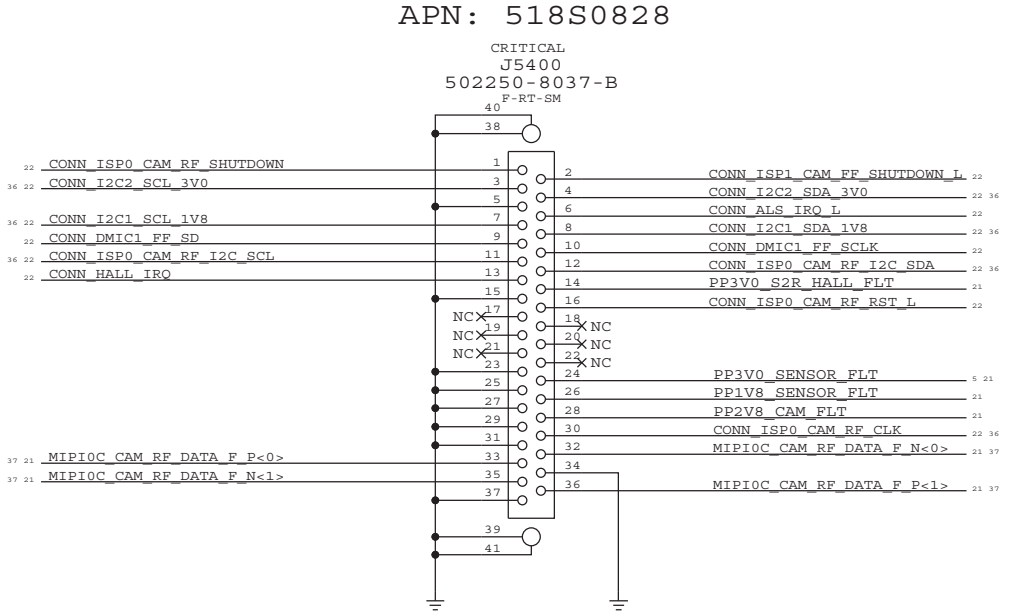
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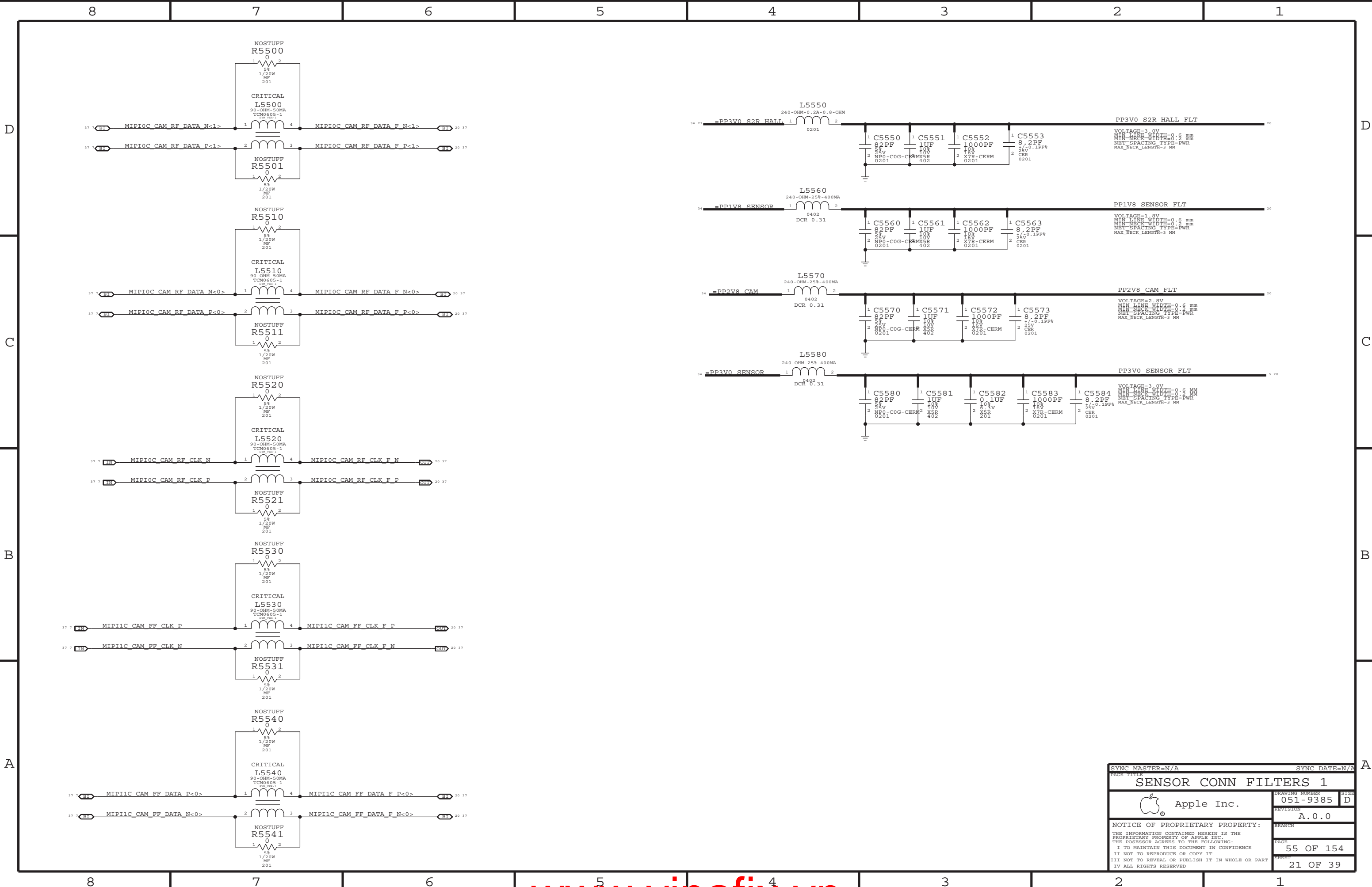
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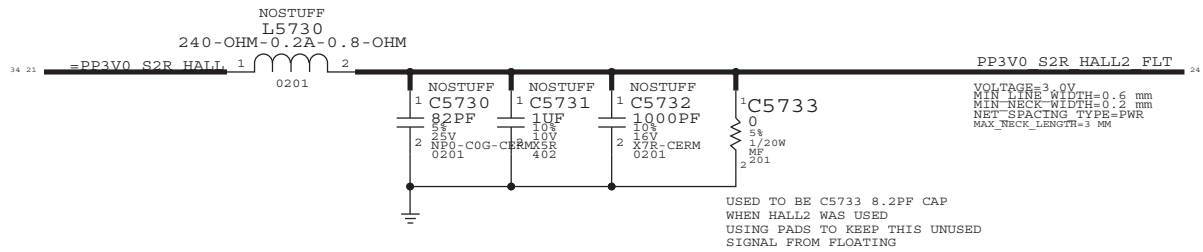
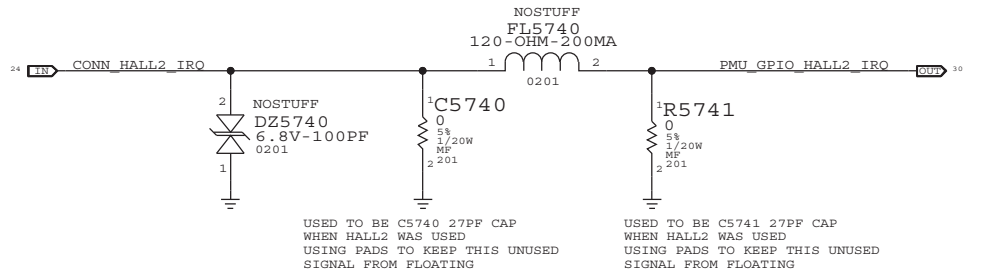
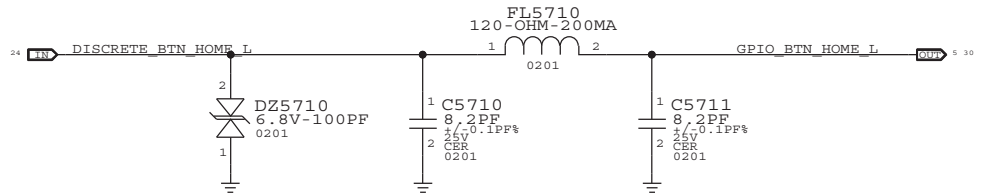
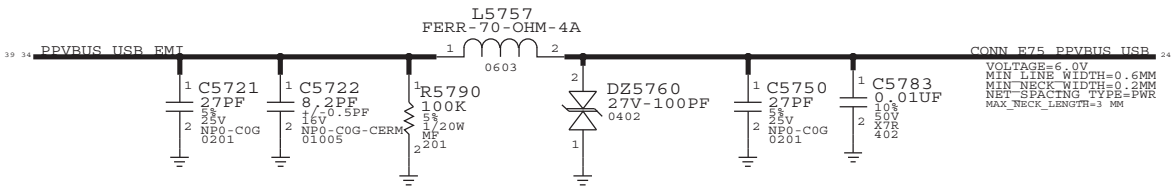
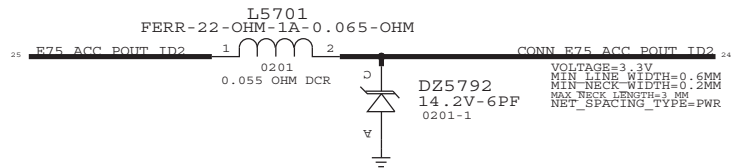
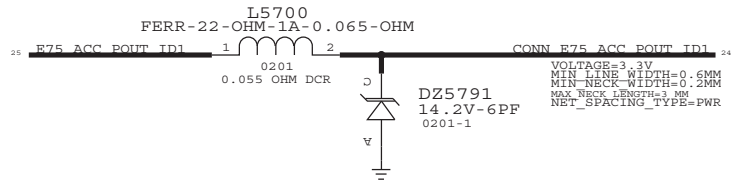
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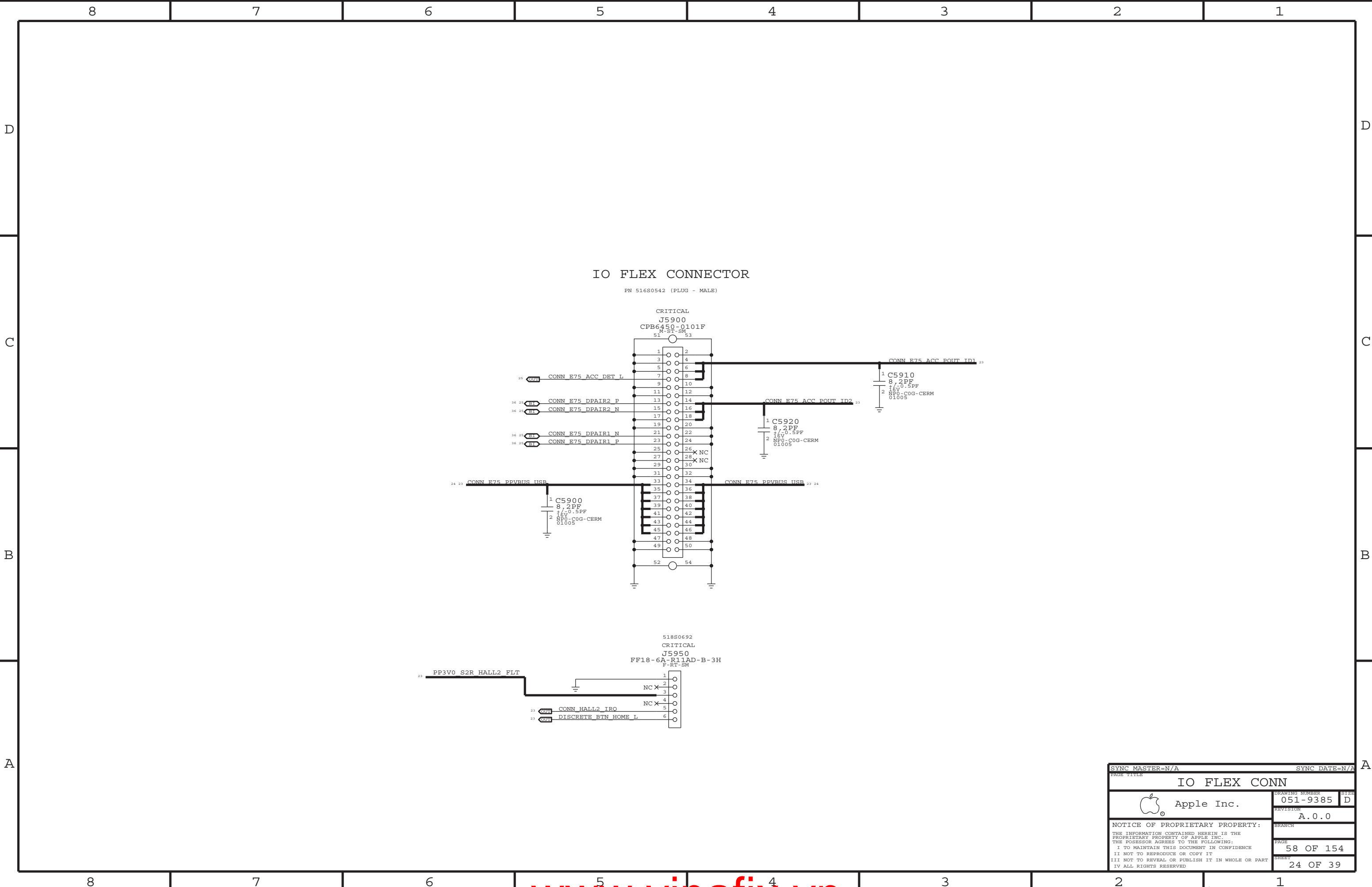
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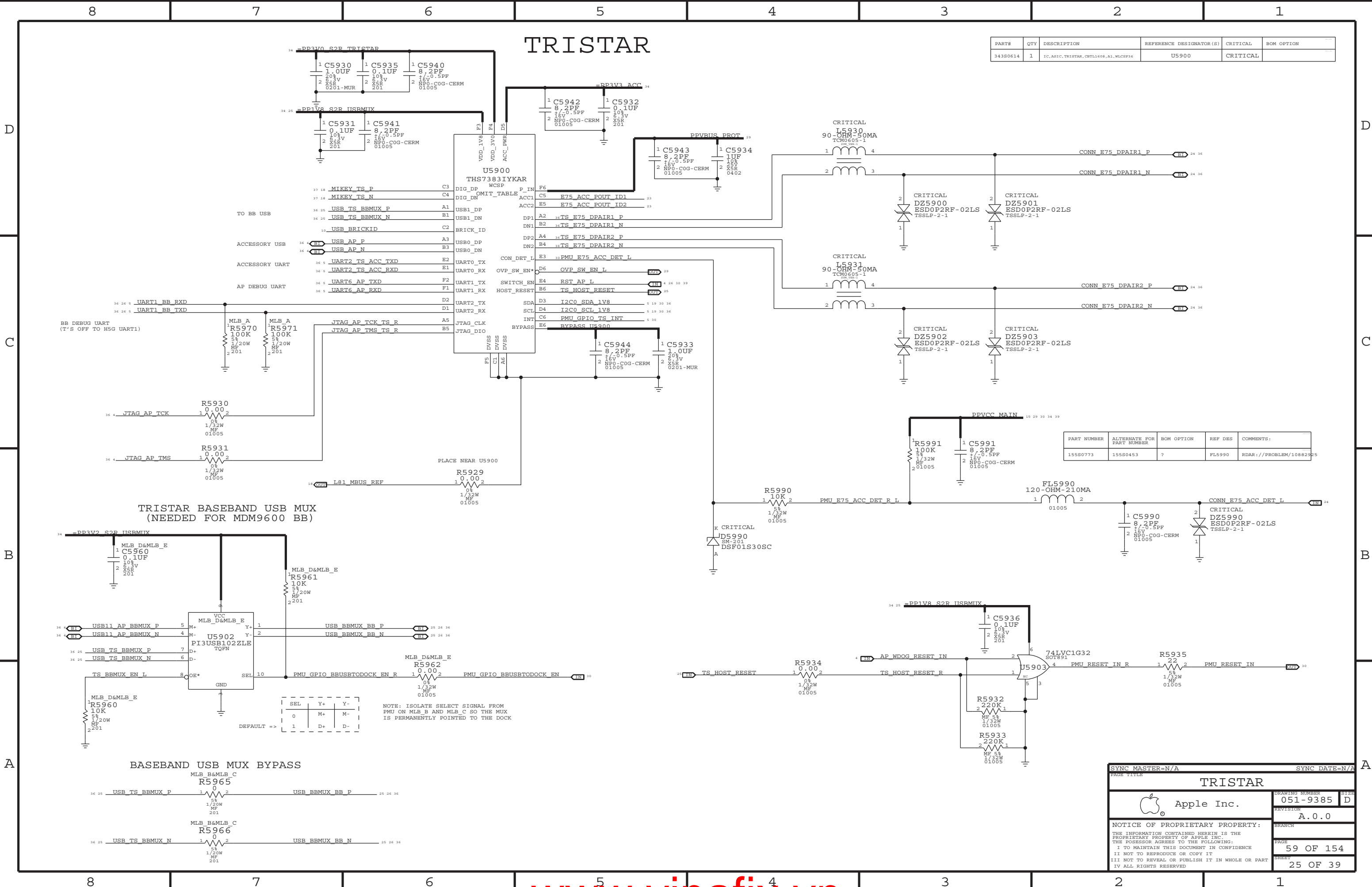


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155S0657	155S0537		FL5710,FL5790	
155S0741	155S0397		L5757	RDAR://PROBLEM/11238841

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		BRANCH	
		PAGE	57 OF 154
		SHEET	23 OF 39



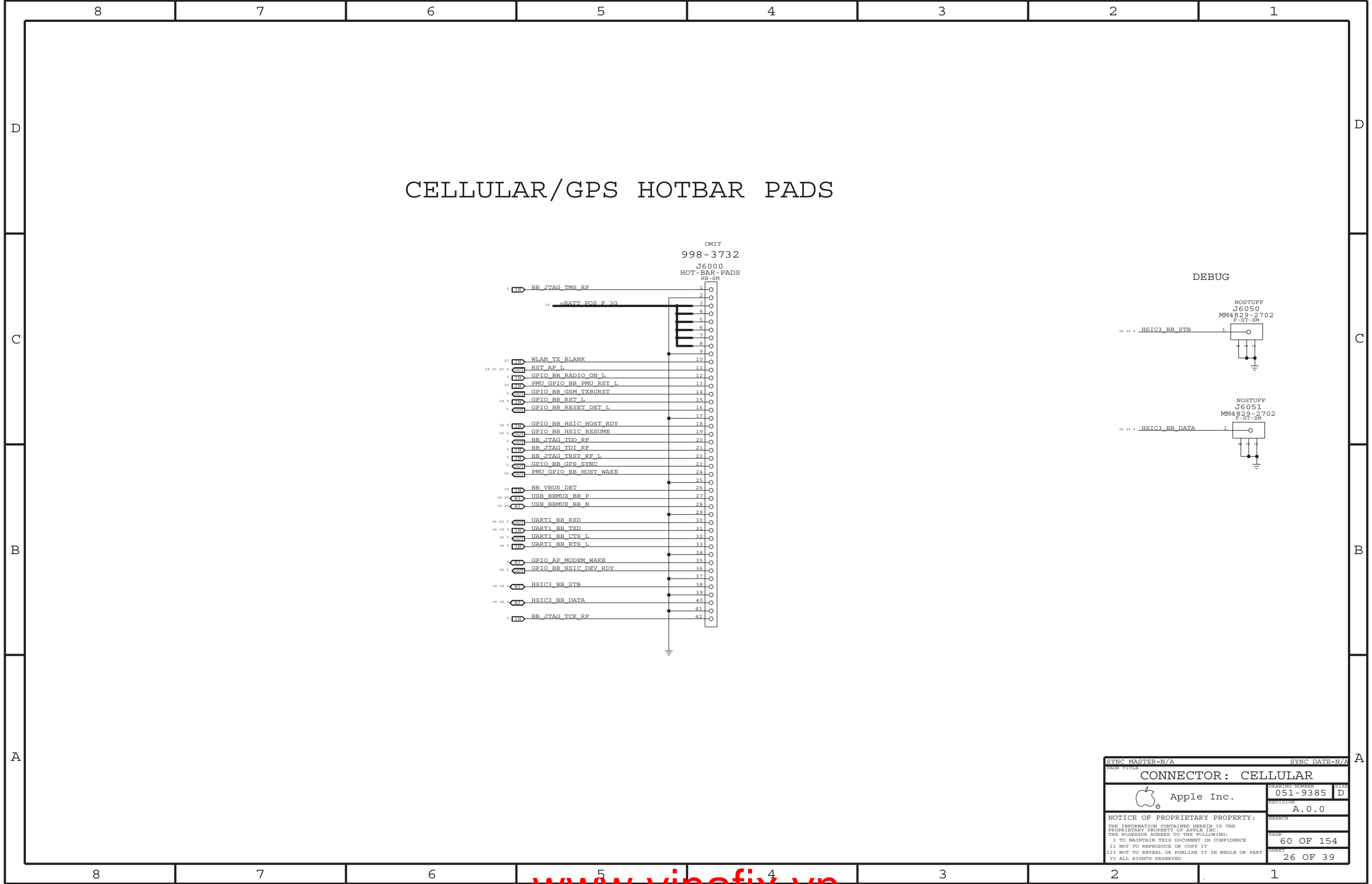
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		PAGE	58 OF 154
		SHEET	24 OF 39



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0614	1	IC, ASIC, TRISTAR, CRTL1608, A1, WLCSP36	U5900	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15550773	15550453	?	FL5990	RDAR://PROBLEM/10882925

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# WLAN/BT

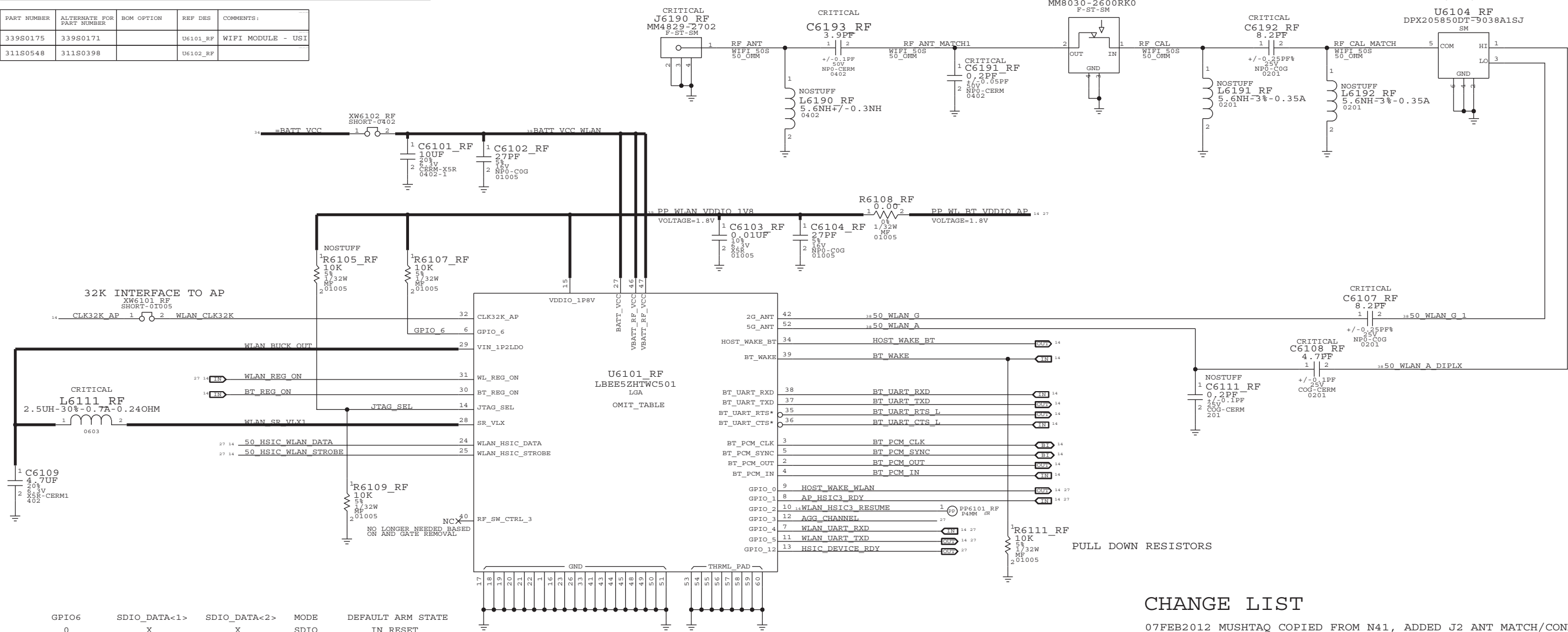
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0171	1	WIFI MODULE - MURATA	U6101_RF	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0175	339S0171		U6101_RF	WIFI MODULE - USI
311S0548	311S0398		U6102_RF	

## ANTENNA CONNECTOR

## CONDUCTED TEST PORT




## CHANGE LIST

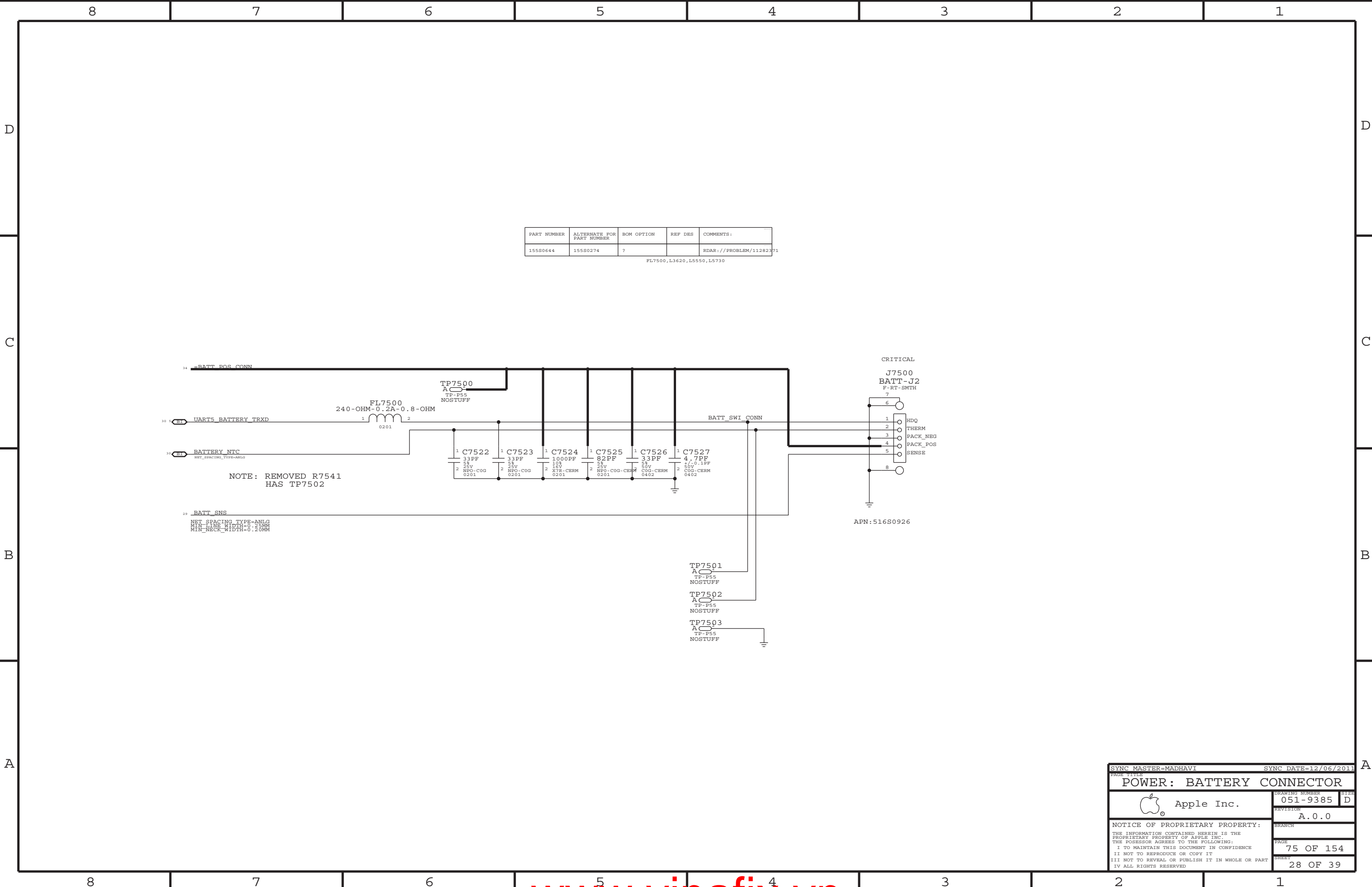
- 07FEB2012 MUSHTAQ COPIED FROM N41, ADDED J2 ANT MATCH/CONN C6107 FROM 20PF TO 8.2PF, C6108 FROM 10PF TO 4.7PF U6104 FROM SOSHIN TO MURATA LFD212G45DS5D355
- 13FEB2012 AMANDA CHANGED OMIT TO OMIT TABLE AND UPDATED BOM OPTION TABLES TO ALTERNATE TABLES REMOVED BOM TABLE FOR C6111\_RF (NOW ALWAYS NOSTUFF)

27 14	WLAN_REG_ON	1	PP6102_RF
27 14	HOST_WAKE_WLAN	1	PP6103_RF
27 14	AP_HSIC3_RDY	1	PP6104_RF
27 14	DEV_HSIC3_RDY	1	PP6105_RF
27 14	WLAN_UART_RXD	1	PP6106_RF
27 14	WLAN_UART_TXD	1	PP6107_RF

27	AGG_CHANNEL	1	PP6109_RF
27 14	50_HSIC_WLAN_DATA	1	PP6110_RF
27 14	50_HSIC_WLAN_STROBE	1	PP6111_RF
27	HSIC_DEVICE_RDY	1	PP6112_RF

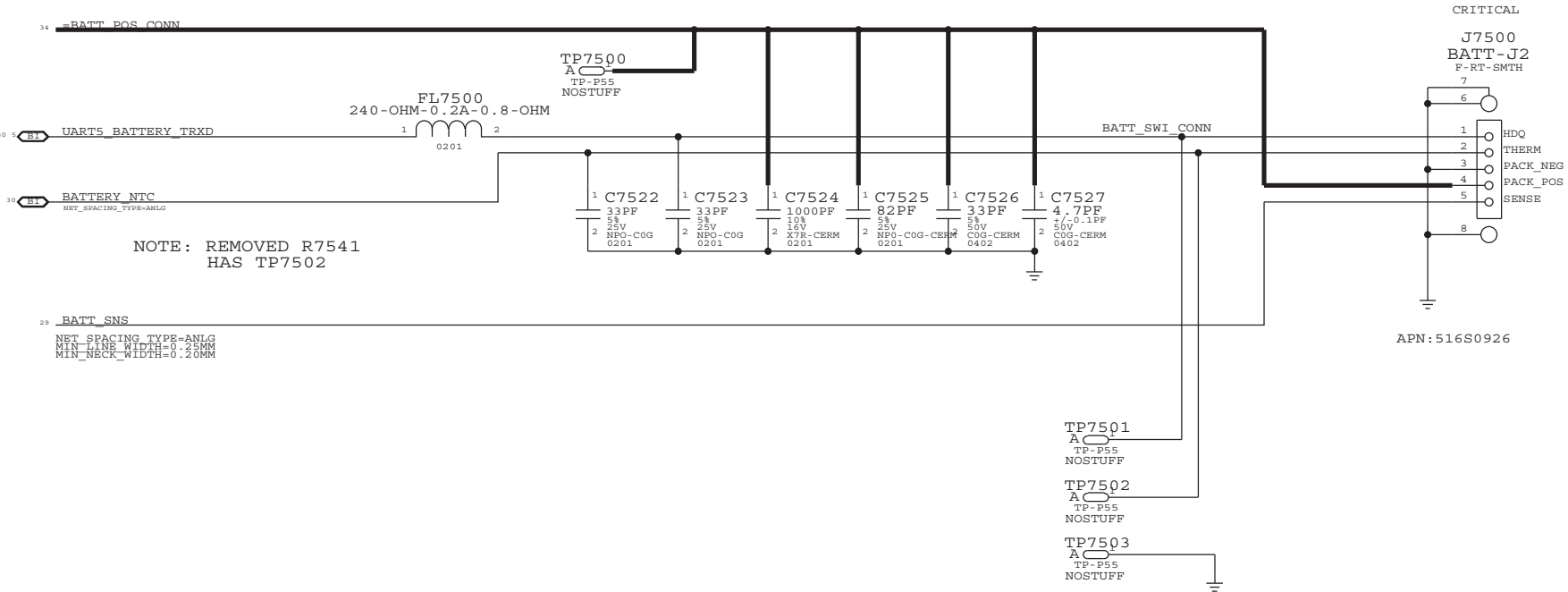
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0274	?		RDAR://PROBLEM/11282371

FL7500, L3620, L5550, L5730



SYNC MASTER=MADHAVI

SYNC DATE=12/06/2011

POWER: BATTERY CONNECTOR

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PAGE

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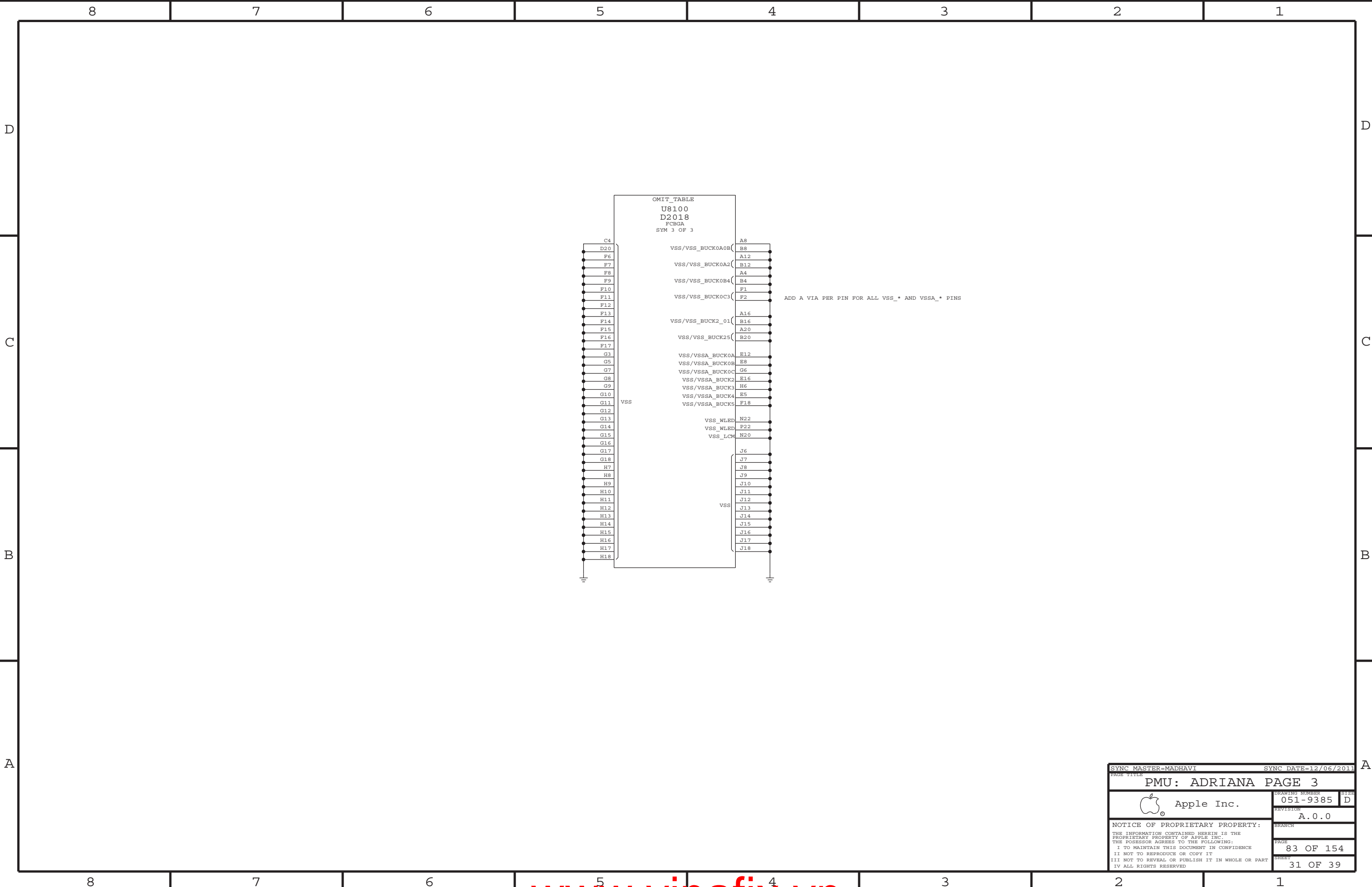
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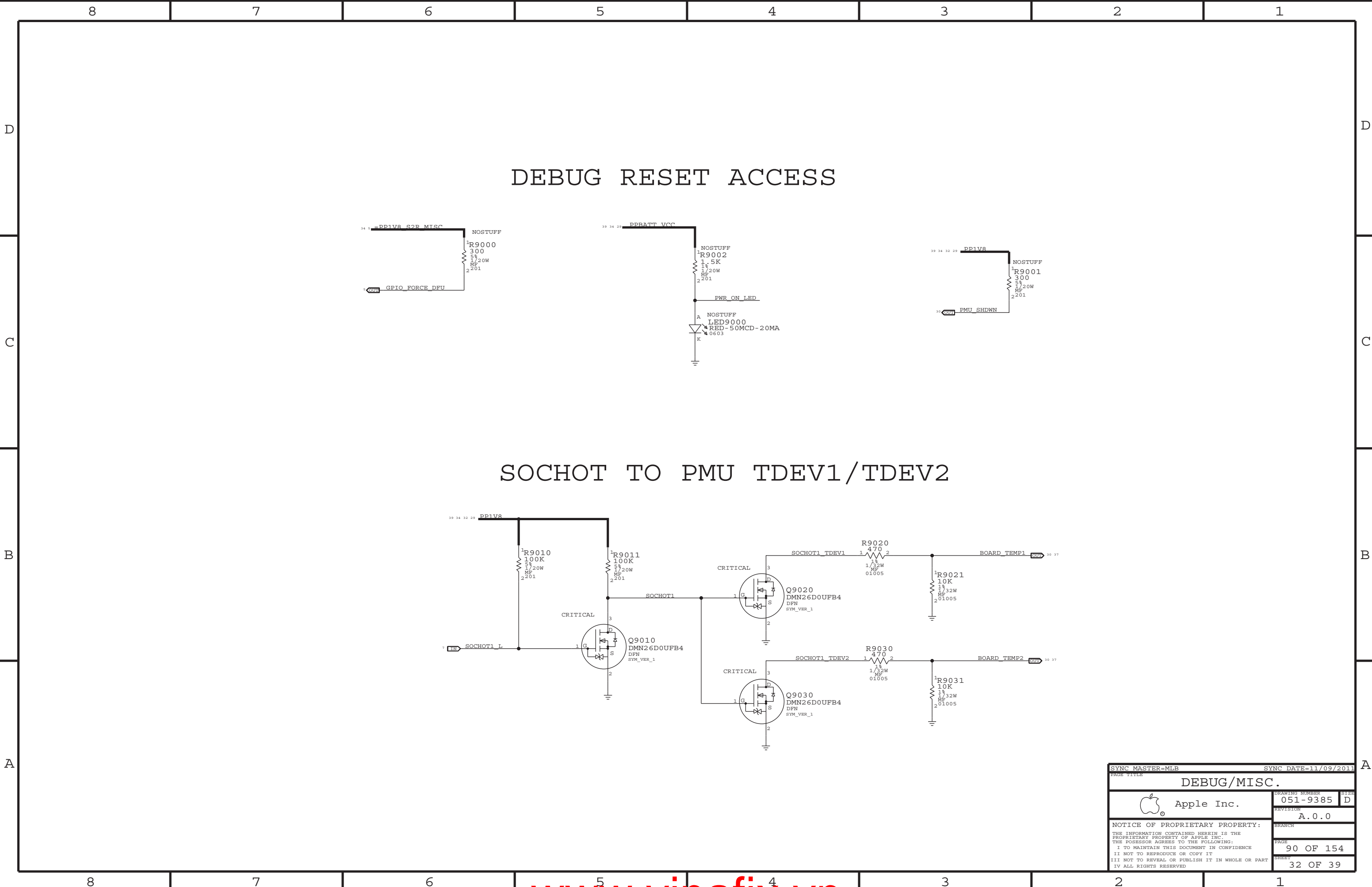
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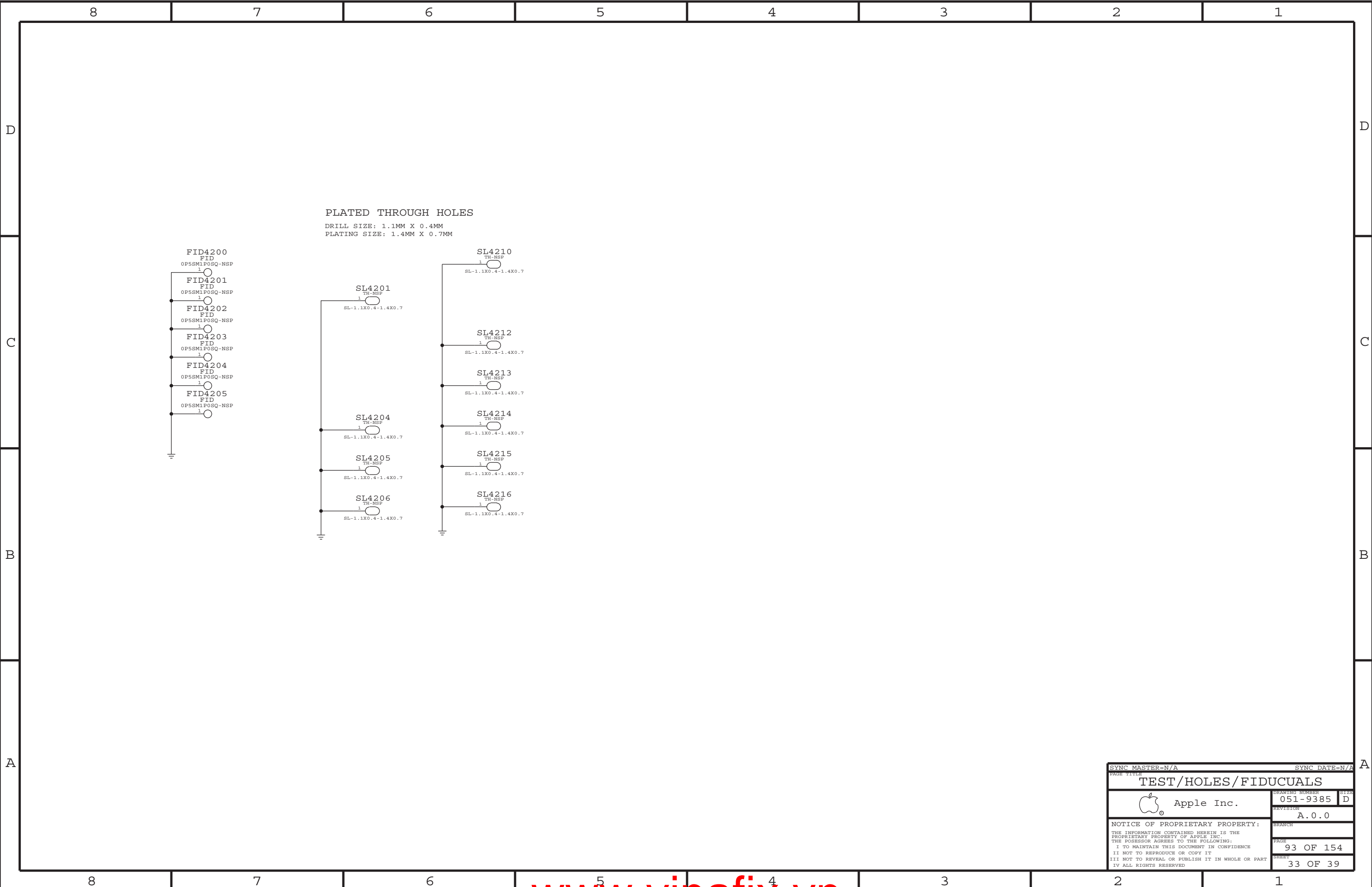
www.vinafix.vn







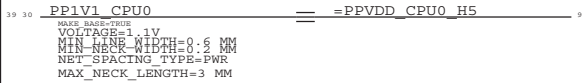






POWER CONNECTIONS

BUCK0A



BUCK0B



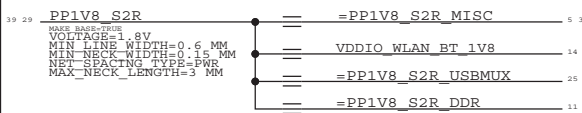
BUCK0C



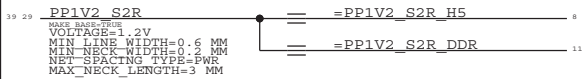
BUCK2



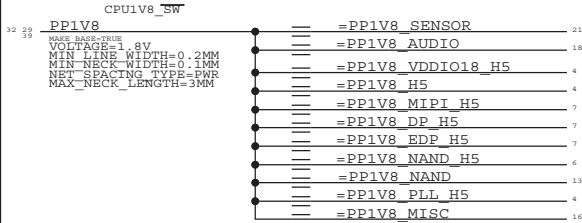
BUCK3



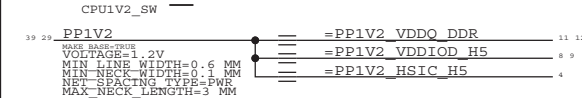
BUCK4



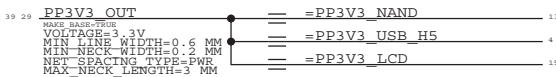
BUCK3\_SW



BUCK4\_SW



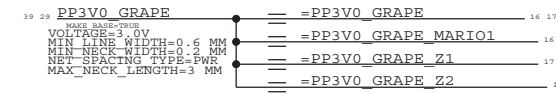
BUCK5



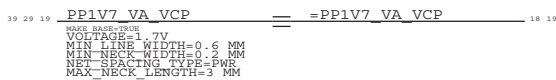
BACKLIGHT BOOST



LDO1



LDO2



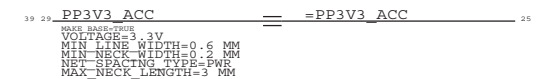
LDO3 (NO LONGER NEEDED)



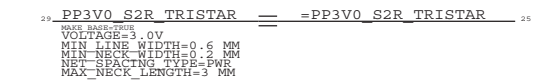
LDO4



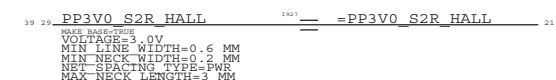
LDO6



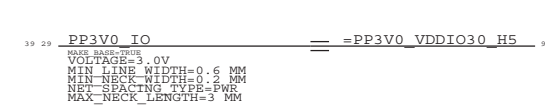
LDO7



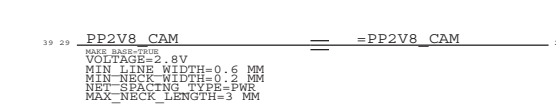
LDO8



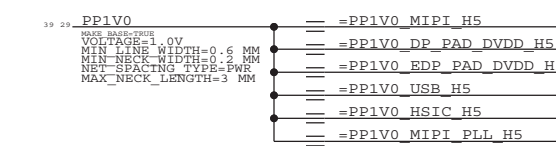
LDO9



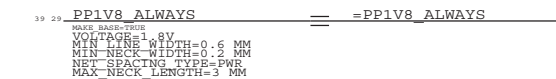
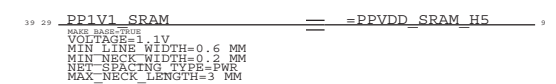
LDO11



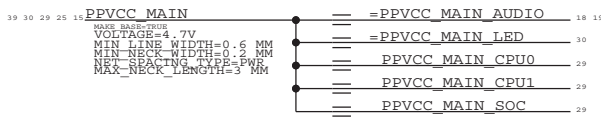
LDO12



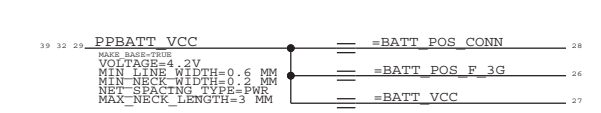
LDO16



CHARGER MAIN



BATTERY



USB POWER INPUT





MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA, BGA06-06, BGA_P4	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	3.0 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES  
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.105 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL2, ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL3, ISL8	Y	0.065 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4, ISL7	Y	0.053 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL5	Y	0.072 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL6	Y	0.059 MM	0.055 MM	3.0 MM		

90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
90_OHM_DIFF	ISL2, ISL9	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL3, ISL8	Y	0.062 MM	0.052 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL4, ISL7	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL5, ISL6	Y	0.052 MM	0.052 MM	=STANDARD	0.105 MM	0.105 MM

DDR 45 OHMS SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_45_OHM_SE	TOP, BOTTOM	Y	0.105 MM	0.105 MM	3.0 MM		
DDR_45_OHM_SE	ISL2	Y	0.055 MM	0.055 MM	3.0 MM		
DDR_45_OHM_SE	ISL3	Y	0.065 MM	0.065 MM	3.0 MM		
DDR_45_OHM_SE	ISL4	Y	0.053 MM	0.053 MM	3.0 MM		
DDR_45_OHM_SE	ISL5, ISL6	Y	0.072 MM	0.072 MM	3.0 MM		
DDR_45_OHM_SE	*	N	0.055 MM	0.055 MM	3.0 MM		

DDR 90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_90_OHM_DIFF	TOP, BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
DDR_90_OHM_DIFF	ISL2	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL3	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL4	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL5, ISL6	Y	0.066 MM	0.066 MM	=STANDARD	0.180 MM	0.180 MM
DDR_90_OHM_DIFF	*	N	0.056 MM	0.056 MM	=STANDARD	0.180 MM	0.180 MM

WIFI PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WIFI_50S	TOP, BOTTOM	Y	0.245 MM	0.2 MM	=STANDARD		
WIFI_50S	*	N	=STANDARD	=STANDARD	=STANDARD		
WIFI_PWR100	*	Y	0.10 MM	0.050 MM	=STANDARD		
WIFI_PWR1000	*	Y	1.00 MM	0.100 MM	=STANDARD		

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.5 MM	0.20 MM	10 MM	0.10 MM	0.10 MM
AUDIO_DIFF	*	Y	0.1 MM	0.09 MM	10 MM	0.10 MM	0.10 MM
LED	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM
TEMP_SENSE	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

TCF VERSION (USING SPACING RULE)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TCF_VERSION	*	0.104 MM	?

0.104 - 11/30/2011

TCF\_VERSION NC\_UART5\_TXD \*ASSIGNING RULE TO NC NET

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?
BGA_P4_SPA	*	0.200 MM	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.050 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.075 MM	?
2:1_SPACING	*	0.100 MM	?
2.5:1_SPACING	*	0.125 MM	?
3:1_SPACING	*	0.150 MM	?
4:1_SPACING	*	0.200 MM	?
5:1_SPACING	*	0.250 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?
0P2_SPACING	*	0.20 MM	?

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	
GND_P1SPACING	*	0.1 MM	
SWITCHNODE	*	0.2 MM	

POWER


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.20 MM	3.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	3.0 MM		
PWR_PMU	*	Y	0.6MM	0.20 MM	3.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
*	*	BGA_P4	BGA_P4_SPA

NOTES:

0.075 MM ~ 3 MIL  
0.089 MM ~ 3.5 MIL  
0.102 MM ~ 4 MIL  
0.114 MM ~ 4.5 MIL  
0.125 MM ~ 5 MIL  
0.140 MM ~ 5.5 MIL  
0.15 MM ~ 6 MIL  
0.18 MM ~ 7 MIL  
0.2 MM ~ 8 MIL  
0.25 MM ~ 10 MIL  
0.3 MM ~ 12 MIL  
0.33 MM ~ 13 MIL  
0.4 MM ~ 16 MIL  
1.0 MM = 39.37 MIL

SYNC MASTER=MIKE		SYNC DATE=11/30/2011	
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		REVISION	A.0.0
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		SHEET	35 OF 39

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	3:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PMU	CLK_50S	CLK	PMU_GPIO_CLK_32K_GRAPE 17 30
PMU	CLK_50S	CLK	PMU_GPIO_CLK_32K_WLAN 14 30
ISP1	CLK_50S	CLK	ISP1_CAM_FF_CLK 7 22
CONN	CLK_50S	CLK	CONN_ISP1_CAM_FF_CLK 20 22
ISP0	CLK_50S	CLK	ISP0_CAM_RF_CLK 7 22
CONN	CLK_50S	CLK	CONN_ISP0_CAM_RF_CLK 20 22
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_MCK 5 36
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R 5 18 36
ISP0	CLK_50S	CLK	ISP0_CAM_RF_CLK_R 7
ISP1	CLK_50S	CLK	ISP1_CAM_FF_CLK_R 7
ISP1	CLK_50S	CLK	ISP1_CAM_FF_C 22
ISP0	CLK_50S	CLK	ISP0_CAM_RF_C 22
ISP1	CLK_50S	CLK	ISP1_CAM_FF_FILT 22
ISP0	CLK_50S	CLK	ISP0_CAM_RF_FILT 22

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
UART2	UART_50S	UART	UART2_TS_ACC_RXD 5 25
UART2	UART_50S	UART	UART2_TS_ACC_TXD 5 25
UART4	UART_50S	UART	UART4_WLAN_RXD 5 14
UART4	UART_50S	UART	UART4_WLAN_TXD 5 14
UART1	UART_50S	UART	UART1_BB_CTS_L 5 26
UART1	UART_50S	UART	UART1_BB_RTS_L 5 26
UART1	UART_50S	UART	UART1_BB_TXD 5 25 26
UART1	UART_50S	UART	UART1_BB_RXD 5 25 26
UART3	UART_50S	UART	UART3_BT_CTS_L 5 14
UART3	UART_50S	UART	UART3_BT_RTS_L 5 14
UART3	UART_50S	UART	UART3_BT_RXD 5 14
UART3	UART_50S	UART	UART3_BT_TXD 5 14
UART6	UART_50S	UART	UART6_AP_RXD 5 25
UART6	UART_50S	UART	UART6_AP_TXD 5 25

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
SPI3	SPT_50S	SPT	SPI3_GRAPE_MISO 5 16
SPI3	SPT_50S	SPT	SPI3_GRAPE_MOSI 5 16
SPI3	SPT_50S	SPT	SPI3_GRAPE_SCLK 5 16
SPI3	SPT_50S	SPT	SPI3_GRAPE_CS_L 5 16
SPI2	SPT_50S	SPT	SPI2_IPC_MISO
SPI2	SPT_50S	SPT	SPI2_IPC_MOSI
SPI2	SPT_50S	SPT	SPI2_IPC_SCLK
SPI2	SPT_50S	SPT	GPIO_BB_HSIC_RESUME 5 26
SPI1	SPT_50S	SPT	SPI1_CODEC_MISO 5 18
SPI1	SPT_50S	SPT	SPI1_CODEC_MOSI 5 18
SPI1	SPT_50S	SPT	SPI1_CODEC_SCLK 5 18
SPI1	SPT_50S	SPT	SPI1_CODEC_CS_L 5 18

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DWI		DWI	DWI_AP_CLK 5 30
DWI		DWI	DWI_AP_DI 5 30
DWI		DWI	DWI_AP_DO 5 30

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
JTAG		JTAG	JTAG_AP_TCK 4 25
JTAG		JTAG	JTAG_AP_TMS 4 25
JTAG		JTAG	JTAG_AP_TDI 4
JTAG		JTAG	TR_JTAG_AP_TDO 4
JTAG		EST	JTAG_AP_TRST_L 4 10 39

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I2C1	I2C_50S	I2C	I2C1_SDA_1V8 5 22
I2C1	I2C_50S	I2C	I2C1_SCL_1V8 5 22
I2C0	I2C_50S	I2C	I2C0_SDA_1V8 5 19 25 30
I2C0	I2C_50S	I2C	I2C0_SCL_1V8 5 19 25 30
I2C2	I2C_50S	I2C	I2C2_SDA_3V0 5 22
I2C2	I2C_50S	I2C	I2C2_SCL_3V0 5 22
ISP0	I2C_50S	I2C	ISP0_CAM_RF_I2C_SCL 7 22
ISP0	I2C_50S	I2C	ISP0_CAM_RF_I2C_SDA 7 22
ISP1	I2C_50S	I2C	ISP1_CAM_FF_I2C_SCL 7 22
ISP1	I2C_50S	I2C	ISP1_CAM_FF_I2C_SDA 7 22
CONN	I2C_50S	I2C	CONN_I2C1_SDA_1V8 20 22
CONN	I2C_50S	I2C	CONN_I2C1_SCL_1V8 20 22
CONN	I2C_50S	I2C	CONN_I2C2_SCL_3V0 20 22
CONN	I2C_50S	I2C	CONN_I2C2_SDA_3V0 20 22
CONN	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SCL 20 22
CONN	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SDA 20 22
CONN	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SCL 20 22
CONN	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SDA 20 22

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
XTAL		CRYSTAL	XTAL_AP_24M_I 4
XTAL		CRYSTAL	XTAL_AP_24M_O 4
XTAL		CRYSTAL	AP_24M_O 4
PMU		CRYSTAL	PMU_XTAL 29
PMU		CRYSTAL	PMU_EXTAL 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_BCLK 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_LRCK 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_DIN 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_DOUT 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_SDOUT 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_MCK 5 36
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R 5 18 36
I2S3	I2S_50S	I2S	I2S3_CODEC_XSP_BCLK 5 18
I2S3	I2S_50S	I2S	I2S3_CODEC_XSP_LRCK 5 18
I2S3	I2S_50S	I2S	I2S3_CODEC_XSP_DIN 5 18
I2S3	I2S_50S	I2S	I2S3_CODEC_XSP_DOUT 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_XSP_SDOUT 5 18
I2S2	I2S_50S	I2S	I2S2_BT_BCLK 5 14
I2S2	I2S_50S	I2S	I2S2_BT_LRCK 5 14
I2S2	I2S_50S	I2S	I2S2_BT_DIN 5 14
I2S2	I2S_50S	I2S	I2S2_BT_DOUT 5 14

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	4:1_SPACING


NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
USB	USB_90D	USB	USB_AP_P 4 25
USB	USB_90D	USB	USB_AP_N 4 25
USB	USB_90D	USB	USB_BBMUX_BB_P 25 26
USB	USB_90D	USB	USB_BBMUX_BB_N 25 26
USB	USB_90D	USB	USB_TS_BBMUX_P 25
USB	USB_90D	USB	USB_TS_BBMUX_N 25
USB	USB_90D	USB	USB11_AP_BBMUX_P 4 25
USB	USB_90D	USB	USB11_AP_BBMUX_N 4 25
CONN	USB_90D	USB	CONN_E75_DPAIR1_P 24 25
CONN	USB_90D	USB	CONN_E75_DPAIR1_N 24 25
CONN	USB_90D	USB	CONN_E75_DPAIR2_P 24 25
CONN	USB_90D	USB	CONN_E75_DPAIR2_N 24 25
TS	USB_90D	USB	TS_E75_DPAIR1_P 25
TS	USB_90D	USB	TS_E75_DPAIR1_N 25
TS	USB_90D	USB	TS_E75_DPAIR2_P 25
TS	USB_90D	USB	TS_E75_DPAIR2_N 25

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC_RDY	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
HSIC3	HSIC	HSIC	HSIC3_BB_DATA 4 26
HSIC3	HSIC	HSIC	HSIC3_BB_STB 4 26
HSIC1	HSIC	HSIC	HSIC1_WLAN_DATA 4 14
HSIC1	HSIC	HSIC	HSIC1_WLAN_STB 4 14
GPIO	HSIC	HSIC_RDY	GPIO_BB_HSIC_DEV_RDY 5 26
GPIO	HSIC	HSIC_RDY	GPIO_BB_HSIC_HOST_RDY 5 26
GPIO	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY 5 14 36
GPIO	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY 5 14 36
GPIO	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_DEV_RDY 5 14

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## MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPIOC	*	*	4:1_SPACING
MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_CLK_P 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_CLK_N 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_P<0> 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_N<0> 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_P<1> 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_N<1> 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_CLK_F_P 20 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_CLK_F_N 20 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_F_P<0> 20 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_F_P<1> 20 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_F_N<1> 20 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_P 7 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_N 7 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_P<0> 7 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_N<0> 7 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_P 20 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_N 20 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_P<0> 20 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_N<0> 20 21

## AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30	AUDIO_DIFF	AUDIO	HP_MIC_P 18
RE30	AUDIO_DIFF	AUDIO	HP_MIC_N 18
RE30	AUDIO_DIFF	AUDIO	L81_AIN2_P 18
RE30	AUDIO_DIFF	AUDIO	L81_AIN2_N 18
RE30	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N_FILT 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P_FILT 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N_FILT 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P_FILT 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P 19
RE30	SPEAKER	AUDIO	SPKR_L_P 19
RE30	SPEAKER	AUDIO	SPKR_L_N 19
RE30	SPEAKER	AUDIO	SPKR_L_CONN_P 19
RE30	SPEAKER	AUDIO	SPKR_L_CONN_N 19
RE30	SPEAKER	AUDIO	SPKR_R_P 19
RE30	SPEAKER	AUDIO	SPKR_R_N 19
RE30	SPEAKER	AUDIO	SPKR_R_CONN_P 19
RE30	SPEAKER	AUDIO	SPKR_R_CONN_N 19
RE30	SPEAKER	AUDIO	SPKR_L_FLR 19
RE30	SPEAKER	AUDIO	SPKR_R_FLR 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_SES_N 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_SES_P 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_SES_N 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_SES_P 19
RE30	USB_90D	USB	MIKEY_TS_P 18 25
RE30	USB_90D	USB	MIKEY_TS_N 18 25
RE30	USB_90D	USB	L81_MBUS_P 18
RE30	USB_90D	USB	L81_MBUS_N 18

## EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF	EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30	EDP_90D	EDP	EDP_AUX_P 7 15
RE30	EDP_90D	EDP	EDP_AUX_N 7 15
RE30	EDP_50S	EDP	EDP_HPD 7 15
RE30	EDP_90D	EDP	EDP_DATA_P<0> 7 15
RE30	EDP_90D	EDP	EDP_DATA_N<0> 7 15
RE30	EDP_90D	EDP	EDP_DATA_P<1> 7 15
RE30	EDP_90D	EDP	EDP_DATA_N<1> 7 15
RE30	EDP_90D	EDP	EDP_DATA_P<2> 7 15
RE30	EDP_90D	EDP	EDP_DATA_N<2> 7 15
RE30	EDP_90D	EDP	EDP_DATA_P<3> 7 15
RE30	EDP_90D	EDP	EDP_DATA_N<3> 7 15
RE30	EDP_90D	EDP	EDP_AUX_EMI_P 15
RE30	EDP_90D	EDP	EDP_AUX_EMI_N 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_P<0> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_N<0> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_P<1> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_N<1> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_P<2> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_N<2> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_P<3> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_N<3> 15
RE30	EDP_90D	EDP	CONN_EDP_AUX_EMI_P 15
RE30	EDP_90D	EDP	CONN_EDP_AUX_EMI_N 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<0> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<0> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<1> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<1> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<2> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<2> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<3> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<3> 15

## BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	3:1_SPACING
LEDB	*	*	3:1_SPACING


ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30	LED	LEDA	LED_IO1_A_R 30
RE30	LED	LEDR	LED_IO1_B_R 30
RE30	LED	LEDA	LED_IO2_A_R 30
RE30	LED	LEDR	LED_IO2_B_R 30
RE30	LED	LEDA	LED_IO3_A_R 30
RE30	LED	LEDR	LED_IO3_B_R 30
RE30	LED	LEDA	LED_IO4_A_R 30
RE30	LED	LEDR	LED_IO4_B_R 30
RE30	LED	LEDA	LED_IO5_A_R 30
RE30	LED	LEDR	LED_IO5_B_R 30
RE30	LED	LEDA	LED_IO6_A_R 30
RE30	LED	LEDR	LED_IO6_B_R 30
RE30	LED	LEDA	LED_IO_1_A 15 30
RE30	LED	LEDR	LED_IO_1_B 15 30
RE30	LED	LEDA	LED_IO_2_A 15 30
RE30	LED	LEDR	LED_IO_2_B 15 30
RE30	LED	LEDA	LED_IO_3_A 15 30
RE30	LED	LEDR	LED_IO_3_B 15 30
RE30	LED	LEDA	LED_IO_4_A 15 30
RE30	LED	LEDR	LED_IO_4_B 15 30
RE30	LED	LEDA	LED_IO_5_A 15 30
RE30	LED	LEDR	LED_IO_5_B 15 30
RE30	LED	LEDA	LED_IO_6_A 15 30
RE30	LED	LEDR	LED_IO_6_B 15 30

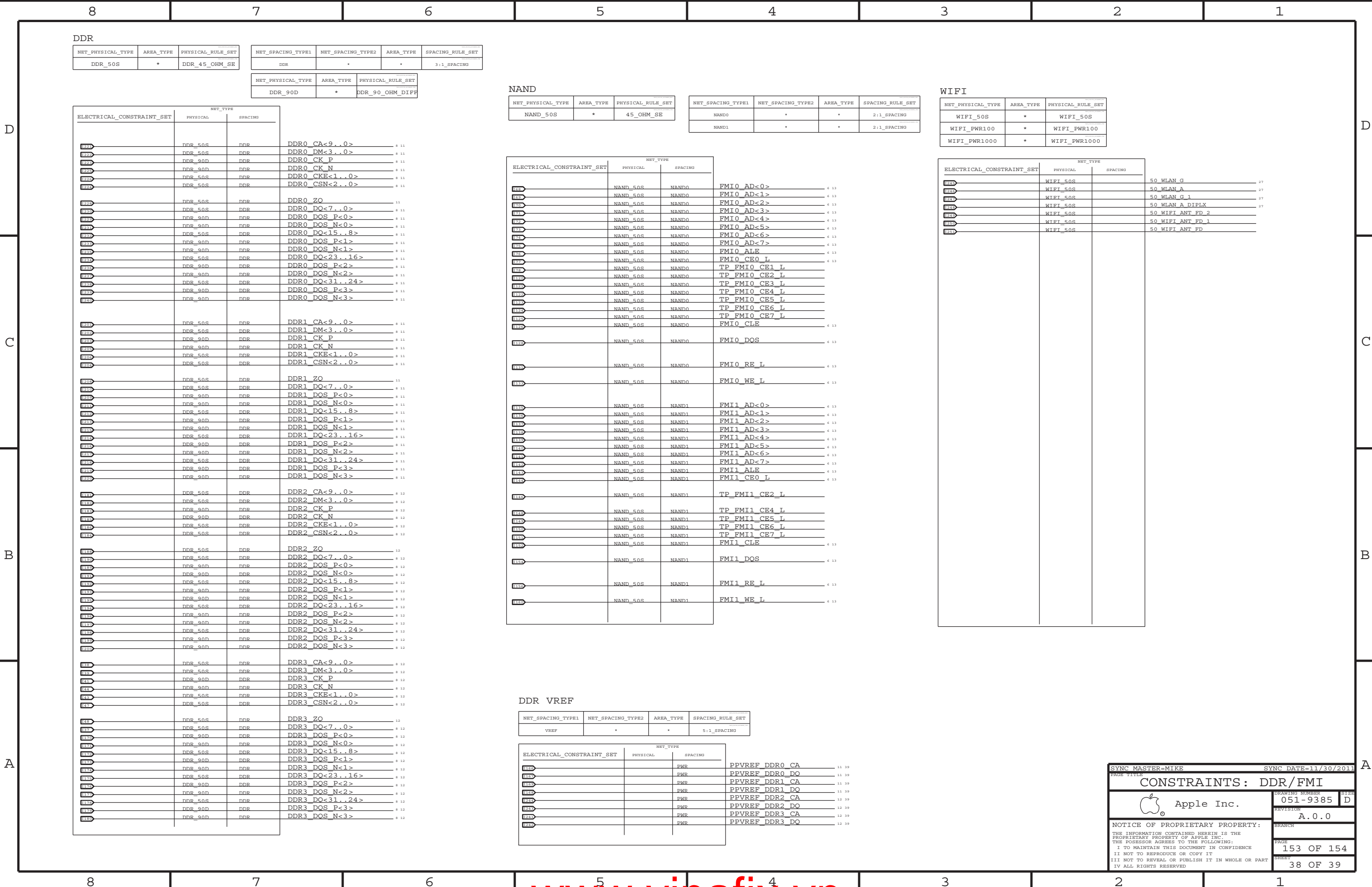
## TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
BOARD_TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30		BOARD_TEMP	BOARD_TEMP1 30 32
RE30		BOARD_TEMP	BOARD_TEMP2 30 32
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_N 30

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DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DDR_45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DDR_90_OHM_DIFP

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND0	*	*	2:1_SPACING
NAND1	*	*	2:1_SPACING

WIFI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	WIFI_50S
WIFI_PWR100	*	WIFI_PWR100
WIFI_PWR1000	*	WIFI_PWR1000

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H220	DDR_50S	DDR	DDR0_CA<9..0>	4 11
H220	DDR_50S	DDR	DDR0_DM<3..0>	4 11
H220	DDR_90D	DDR	DDR0_CK_P	4 11
H220	DDR_90D	DDR	DDR0_CK_N	4 11
H220	DDR_50S	DDR	DDR0_CKE<1..0>	4 11
H220	DDR_50S	DDR	DDR0_CSN<2..0>	4 11
H220	DDR_50S	DDR	DDR0_ZO	11
H220	DDR_50S	DDR	DDR0_DQ<7..0>	4 11
H220	DDR_90D	DDR	DDR0_DQS_P<0>	4 11
H220	DDR_90D	DDR	DDR0_DQS_N<0>	4 11
H220	DDR_50S	DDR	DDR0_DQ<15..8>	4 11
H220	DDR_90D	DDR	DDR0_DQS_P<1>	4 11
H220	DDR_90D	DDR	DDR0_DQS_N<1>	4 11
H220	DDR_50S	DDR	DDR0_DQ<23..16>	4 11
H220	DDR_90D	DDR	DDR0_DQS_P<2>	4 11
H220	DDR_90D	DDR	DDR0_DQS_N<2>	4 11
H220	DDR_50S	DDR	DDR0_DQ<31..24>	4 11
H220	DDR_90D	DDR	DDR0_DQS_P<3>	4 11
H220	DDR_90D	DDR	DDR0_DQS_N<3>	4 11
H200	DDR_50S	DDR	DDR1_CA<9..0>	4 11
H200	DDR_50S	DDR	DDR1_DM<3..0>	4 11
H200	DDR_90D	DDR	DDR1_CK_P	4 11
H200	DDR_90D	DDR	DDR1_CK_N	4 11
H200	DDR_50S	DDR	DDR1_CKE<1..0>	4 11
H200	DDR_50S	DDR	DDR1_CSN<2..0>	4 11
H200	DDR_50S	DDR	DDR1_ZO	11
H200	DDR_50S	DDR	DDR1_DQ<7..0>	4 11
H200	DDR_90D	DDR	DDR1_DQS_P<0>	4 11
H200	DDR_90D	DDR	DDR1_DQS_N<0>	4 11
H200	DDR_50S	DDR	DDR1_DQ<15..8>	4 11
H200	DDR_90D	DDR	DDR1_DQS_P<1>	4 11
H200	DDR_90D	DDR	DDR1_DQS_N<1>	4 11
H200	DDR_50S	DDR	DDR1_DQ<23..16>	4 11
H200	DDR_90D	DDR	DDR1_DQS_P<2>	4 11
H200	DDR_90D	DDR	DDR1_DQS_N<2>	4 11
H200	DDR_50S	DDR	DDR1_DQ<31..24>	4 11
H200	DDR_90D	DDR	DDR1_DQS_P<3>	4 11
H200	DDR_90D	DDR	DDR1_DQS_N<3>	4 11
H180	DDR_50S	DDR	DDR2_CA<9..0>	4 12
H180	DDR_50S	DDR	DDR2_DM<3..0>	4 12
H180	DDR_90D	DDR	DDR2_CK_P	4 12
H180	DDR_90D	DDR	DDR2_CK_N	4 12
H180	DDR_50S	DDR	DDR2_CKE<1..0>	4 12
H180	DDR_50S	DDR	DDR2_CSN<2..0>	4 12
H180	DDR_50S	DDR	DDR2_ZO	12
H180	DDR_50S	DDR	DDR2_DQ<7..0>	4 12
H180	DDR_90D	DDR	DDR2_DQS_P<0>	4 12
H180	DDR_90D	DDR	DDR2_DQS_N<0>	4 12
H180	DDR_50S	DDR	DDR2_DQ<15..8>	4 12
H180	DDR_90D	DDR	DDR2_DQS_P<1>	4 12
H180	DDR_90D	DDR	DDR2_DQS_N<1>	4 12
H180	DDR_50S	DDR	DDR2_DQ<23..16>	4 12
H180	DDR_90D	DDR	DDR2_DQS_P<2>	4 12
H180	DDR_90D	DDR	DDR2_DQS_N<2>	4 12
H180	DDR_50S	DDR	DDR2_DQ<31..24>	4 12
H180	DDR_90D	DDR	DDR2_DQS_P<3>	4 12
H180	DDR_90D	DDR	DDR2_DQS_N<3>	4 12
H160	DDR_50S	DDR	DDR3_CA<9..0>	4 12
H160	DDR_50S	DDR	DDR3_DM<3..0>	4 12
H160	DDR_90D	DDR	DDR3_CK_P	4 12
H160	DDR_90D	DDR	DDR3_CK_N	4 12
H160	DDR_50S	DDR	DDR3_CKE<1..0>	4 12
H160	DDR_50S	DDR	DDR3_CSN<2..0>	4 12
H160	DDR_50S	DDR	DDR3_ZO	12
H160	DDR_50S	DDR	DDR3_DQ<7..0>	4 12
H160	DDR_90D	DDR	DDR3_DQS_P<0>	4 12
H160	DDR_90D	DDR	DDR3_DQS_N<0>	4 12
H160	DDR_50S	DDR	DDR3_DQ<15..8>	4 12
H160	DDR_90D	DDR	DDR3_DQS_P<1>	4 12
H160	DDR_90D	DDR	DDR3_DQS_N<1>	4 12
H160	DDR_50S	DDR	DDR3_DQ<23..16>	4 12
H160	DDR_90D	DDR	DDR3_DQS_P<2>	4 12
H160	DDR_90D	DDR	DDR3_DQS_N<2>	4 12
H160	DDR_50S	DDR	DDR3_DQ<31..24>	4 12
H160	DDR_90D	DDR	DDR3_DQS_P<3>	4 12
H160	DDR_90D	DDR	DDR3_DQS_N<3>	4 12

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
			FMIO_AD<0>	6 13
H060	NAND_50S	NAND0	FMIO_AD<1>	6 13
H060	NAND_50S	NAND0	FMIO_AD<2>	6 13
H060	NAND_50S	NAND0	FMIO_AD<3>	6 13
H060	NAND_50S	NAND0	FMIO_AD<4>	6 13
H060	NAND_50S	NAND0	FMIO_AD<5>	6 13
H060	NAND_50S	NAND0	FMIO_AD<6>	6 13
H060	NAND_50S	NAND0	FMIO_AD<7>	6 13
H060	NAND_50S	NAND0	FMIO_ALE	6 13
H060	NAND_50S	NAND0	FMIO_CE0_L	6 13
H060	NAND_50S	NAND0	TP FMIO CE1_L	
H060	NAND_50S	NAND0	TP FMIO CE2_L	
H060	NAND_50S	NAND0	TP FMIO CE3_L	
H060	NAND_50S	NAND0	TP FMIO CE4_L	
H060	NAND_50S	NAND0	TP FMIO CE5_L	
H060	NAND_50S	NAND0	TP FMIO CE6_L	
H060	NAND_50S	NAND0	TP FMIO CE7_L	
H060	NAND_50S	NAND0	FMIO_CLE	6 13
H060	NAND_50S	NAND0	FMIO_DQS	6 13
H060	NAND_50S	NAND0	FMIO_RE_L	6 13
H060	NAND_50S	NAND0	FMIO_WE_L	6 13
H080	NAND_50S	NAND1	FMI1_AD<0>	6 13
H080	NAND_50S	NAND1	FMI1_AD<1>	6 13
H080	NAND_50S	NAND1	FMI1_AD<2>	6 13
H080	NAND_50S	NAND1	FMI1_AD<3>	6 13
H080	NAND_50S	NAND1	FMI1_AD<4>	6 13
H080	NAND_50S	NAND1	FMI1_AD<5>	6 13
H080	NAND_50S	NAND1	FMI1_AD<6>	6 13
H080	NAND_50S	NAND1	FMI1_AD<7>	6 13
H080	NAND_50S	NAND1	FMI1_ALE	6 13
H080	NAND_50S	NAND1	FMI1_CE0_L	6 13
H080	NAND_50S	NAND1	TP_FMI1_CE2_L	
H080	NAND_50S	NAND1	TP_FMI1_CE4_L	
H080	NAND_50S	NAND1	TP_FMI1_CE5_L	
H080	NAND_50S	NAND1	TP_FMI1_CE6_L	
H080	NAND_50S	NAND1	TP_FMI1_CE7_L	
H080	NAND_50S	NAND1	FMI1_CLE	6 13
H080	NAND_50S	NAND1	FMI1_DQS	6 13
H080	NAND_50S	NAND1	FMI1_RE_L	6 13
H080	NAND_50S	NAND1	FMI1_WE_L	6 13

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
H240	WIFI_50S	50 WLAN_G
H240	WIFI_50S	50 WLAN_A
H240	WIFI_50S	50 WLAN_G_1
H240	WIFI_50S	50 WLAN_A DIPLX
H240	WIFI_50S	50 WIFI ANT FD 2
H240	WIFI_50S	50 WIFI ANT FD 1
H240	WIFI_50S	50 WIFI ANT FD

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H040		PWR	PPVREF_DDR0_CA	11 39
H040		PWR	PPVREF_DDR0_DO	11 39
H040		PWR	PPVREF_DDR1_CA	11 39
H040		PWR	PPVREF_DDR1_DO	11 39
H040		PWR	PPVREF_DDR2_CA	12 39
H040		PWR	PPVREF_DDR2_DO	12 39
H040		PWR	PPVREF_DDR3_CA	12 39
H040		PWR	PPVREF_DDR3_DO	12 39

SYNC MASTER=MIKE

SYNC DATE=11/30/2011

CONSTRAINTS: DDR/FMI

Apple Inc.

DRAWING NUMBER

051-9385

SIZE

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REVISION

A.0.0

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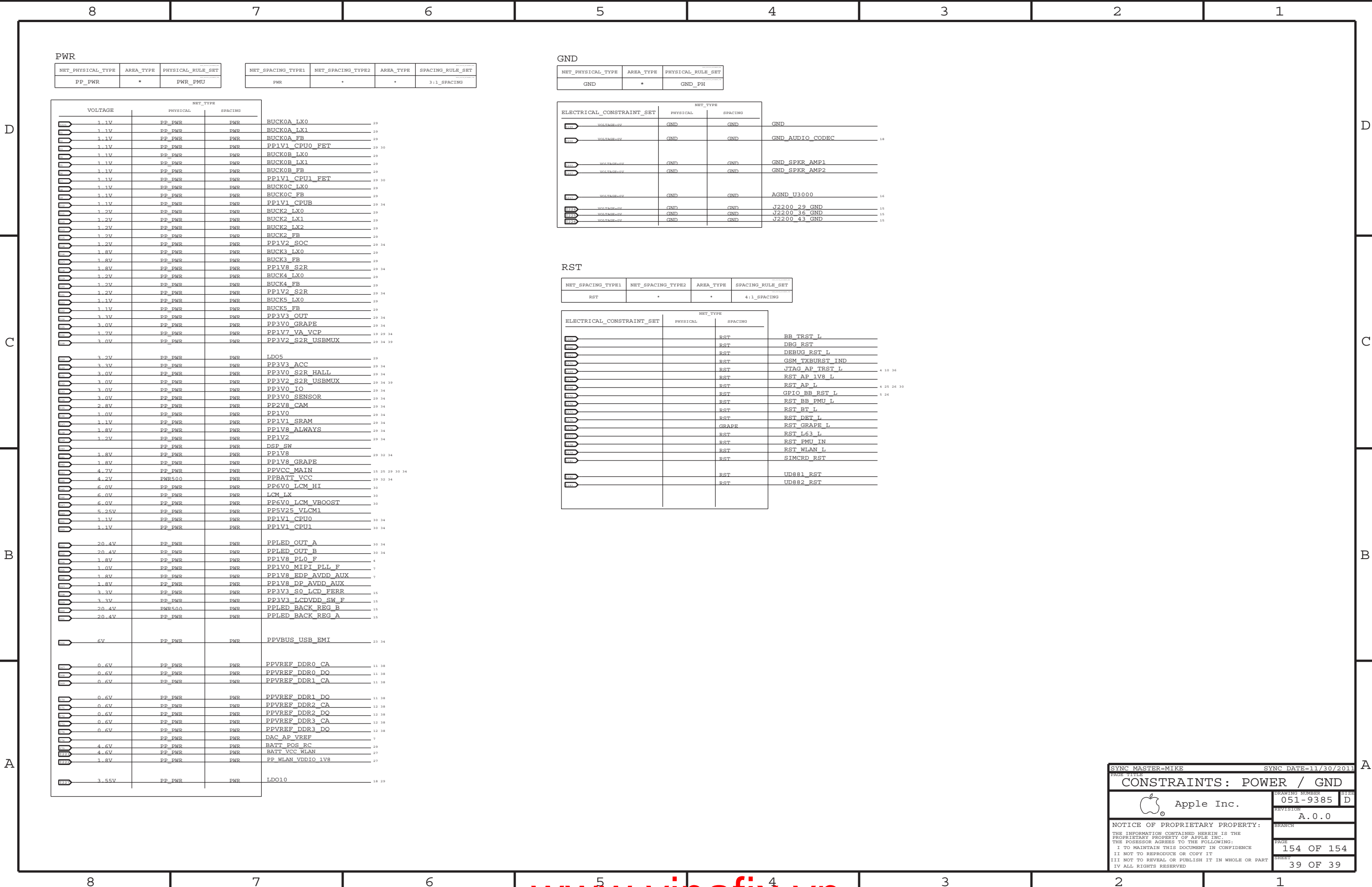
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PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PP_PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_PH

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	V01_TAGE+0V	GND	GND	GND
	V01_TAGE+0V	GND	GND	GND_AUDIO_CODEC
	V01_TAGE+0V	GND	GND	GND_SPKR_AMP1
	V01_TAGE+0V	GND	GND	GND_SPKR_AMP2
	V01_TAGE+0V	GND	GND	AGND_U3000
	V01_TAGE+0V	GND	GND	J2200_29_GND
	V01_TAGE+0V	GND	GND	J2200_36_GND
	V01_TAGE+0V	GND	GND	J2200_43_GND

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING


ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U155		RST	BB_TRST_L	
U156		RST	DBG_RST	
U157		RST	DEBUG_RST_L	
U158		RST	GSM_TXBURST_IND	
U159		RST	JTAG_AP_TRST_L	4 10 36
U160		RST	RST_AP_1V8_L	
U161		RST	RST_AP_L	
U162		RST	GPIO_BB_RST_L	4 25 26 30
U163		RST	RST_BB_PMU_L	5 26
U164		RST	RST_BT_L	
U165		RST	RST_DET_L	
U166		GRAPE	RST_GRAPE_L	
U167		RST	RST_L63_L	
U168		RST	RST_PMU_IN	
U169		RST	RST_WLAN_L	
U170		RST	SIMCRD_RST	
U171		RST	UD881_RST	
U172		RST	UD882_RST	

SYNC MASTER=MIKE

SYNC DATE=11/30/2011

PAGE TITLE

CONSTRAINTS: POWER / GND

 Apple Inc.

DRAWING NUMBER  
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REVISION  
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