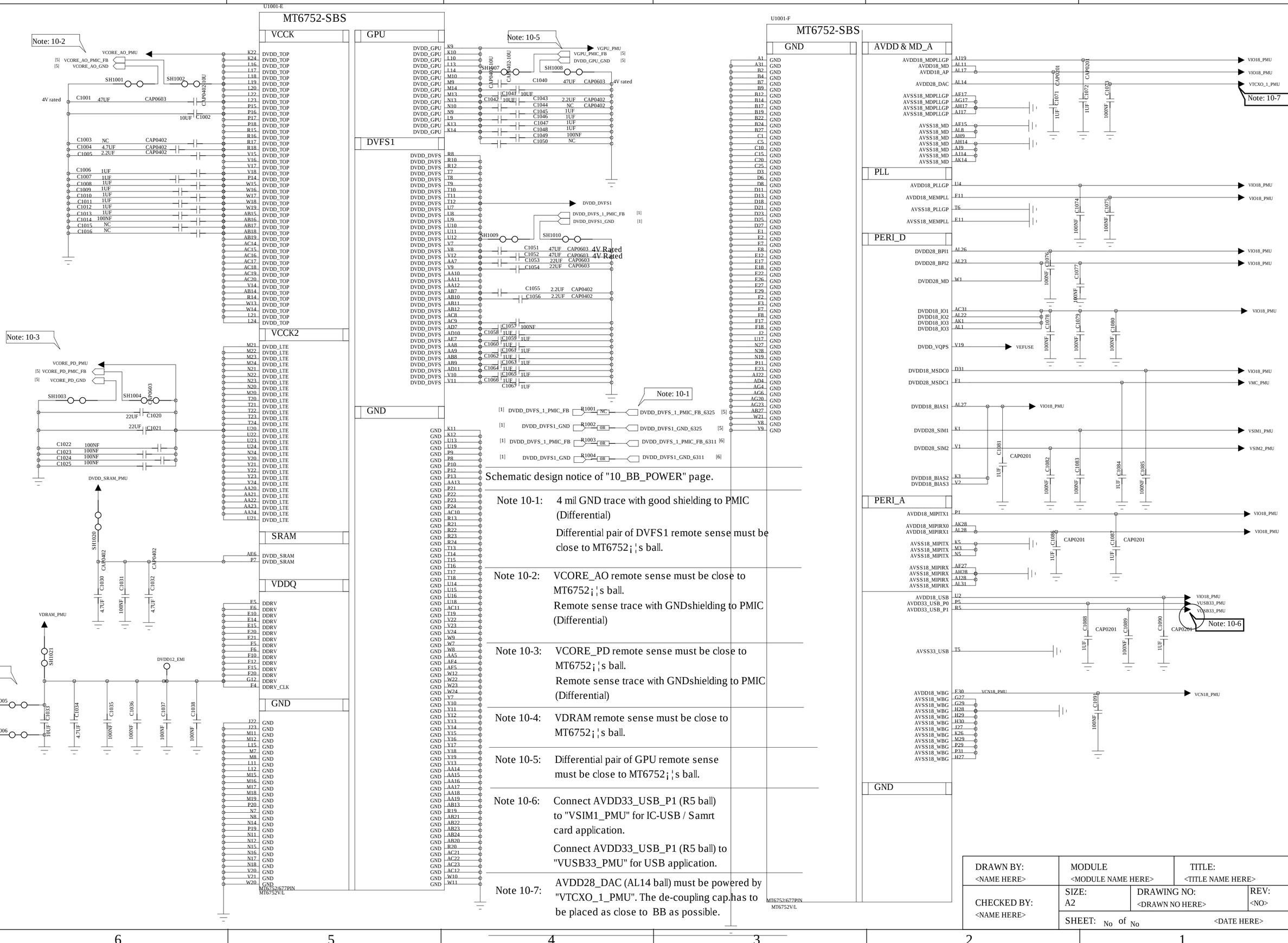


Schematic design notice of "10_BB_POWER" page.

Note 10-1: 4 mil GND trace with good shielding to PMIC (Differential)

Differential pair of DVFS1 remote sense must be close to MT6752¡¦s ball.

Note 10-2: VCORE_AO remote sense must be close to MT6752¡¦s ball.

Remote sense trace with GNDshielding to PMIC (Differential)

Note 10-3: VCORE_PD remote sense must be close to MT6752¡¦s ball.

Remote sense trace with GNDshielding to PMIC (Differential)

Note 10-4: VDRAM remote sense must be close to MT6752¡¦s ball.

Note 10-5: Differential pair of GPU remote sense must be close to MT6752¡¦s ball.

Note 10-6: Connect AVDD33_USB_P1 (R5 ball) to "VSIM1_PMU" for IC-USB / Samrt card application.

Connect AVDD33_USB_P1 (R5 ball) to "VUSB33_PMU" for USB application.

Note 10-7: AVDD28_DAC (AL14 ball) must be powered by "VTCXO_1_PMU". The de-coupling cap.has to be placed as close to BB as possible.

| | | | |
|---|---|---|---|
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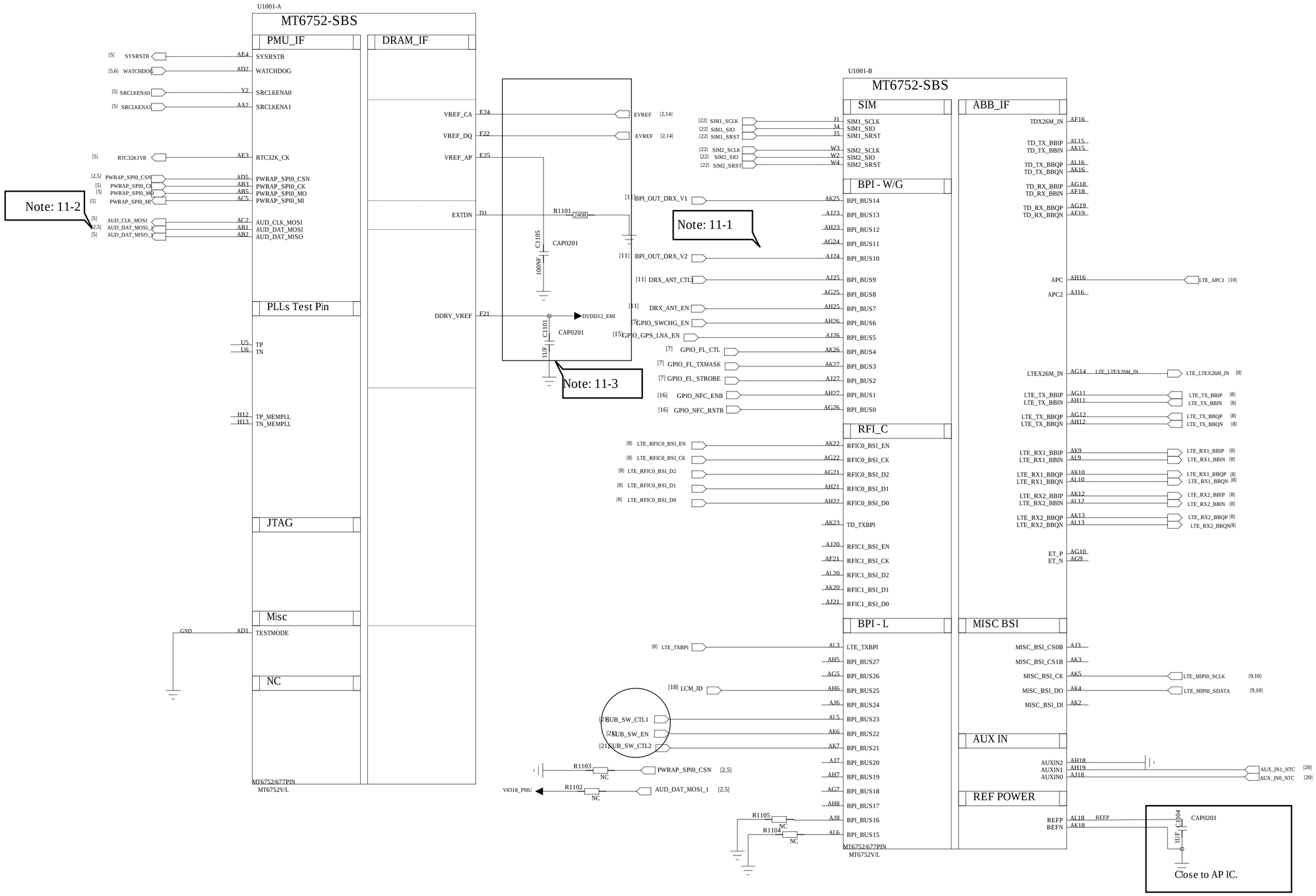



| PWRAP_SPI0_CSN | AUD_DAT_MOSI | JTAG |
|---|---|---|
| HI | LO | N/A GPIO default |
| HI | HI | SPI_CSB/SPI_CLK/SPI_MO/SPI_MI |
| LO | LO | CAM_CLK0/CAM_RST0/CAM_RST1/CAM_PDN0 |
| LO | HI | MSDC1_CLK/MSDC1_CMD/MSDC1_DAT0/MSDC1_DAT1 |

Schematic design notice of "11_BB_1" page.

| | |
|---|---|
| Note 11-1: | The BPI_BUS0~BPI_BUS9 are capable of 2.8V I/O ,according to the input of DVDD28_BPI1 and DVDD28_BPI2 |
| Note 11-2: | PWRAP_SPI0_CSN and AUD_DAT_MOSI are JTAG feature in bootstrap. |
| Note 11-3: | The de-coupling cap. of DRAM VREF have to be placed as close to BB as possible. |

U1001-C

## MT6752-SBS

### CSI

| | | | |
|---|---|---|---|
| [19] RCP | AE26 | RCP | |
| [19] RCN | AE27 | RCN | |
| [19] RDP0 | AE31 | RDP0 | |
| [19] RDN0 | AE30 | RDN0 | |
| [19] RDP1 | AE30 | RDP1 | |
| [19] RDN1 | AF31 | RDN1 | |
| [19] RDP2 | AE28 | RDP2 | |
| [19] RDN2 | AF29 | RDN2 | |
| [19] RDP3 | AH30 | RDP3 | |
| [19] RDN3 | AG30 | RDN3 | |
| [19] RCP_A | AH29 | RCP_A | |
| [19] RCN_A | AG29 | RCN_A | |
| [19] RDP0_A | AH31 | RDP0_A | |
| [19] RDN0_A | AJ31 | RDN0_A | |
| [19] RDP1_A | AK30 | RDP1_A | |
| [19] RDN1_A | AJ30 | RDN1_A | |
| | AK29 | RDP2_A | |
| | AJ29 | RDN2_A | |
| | AL29 | RDP3_A | |
| | AL30 | RDN3_A | |

### DSI

| | | | |
|---|---|---|---|
| TCP | M5 | TCP | [18] |
| TCN | L5 | TCN | [18] |
| TDP0 | M4 | TDP0 | [18] |
| TDN0 | N4 | TDN0 | [18] |
| TDP1 | N3 | TDP1 | [18] |
| TDN1 | N2 | TDN1 | [18] |
| TDP2 | M1 | TDP2 | [18] |
| TDN2 | M2 | TDN2 | [18] |
| TDP3 | L2 | TDP3 | [18] |
| TDN3 | K2 | TDN3 | [18] |

VRT — N1 — MIPI_VRT — R1227 +/-1% 1.5K

| | | | |
|---|---|---|---|
| DISP_PWM | AG1 | DISP_PWM0 | [7] |
| LCM_RST | AE2 | LCM_RST | [18] |
| DSI_TE | AE1 | DSI_TE | [18] |

| | | | |
|---|---|---|---|
| [17] EINT_EAR | AC29 | CMPDAT0 | |
| [20] EINT_A+GYRO | AC28 | CMPDAT1 | |
| [7] EINT_CHG_STAT | AC27 | CMPCLK | |
| [19] CAM_RST0_CLK | AD28 | CAM_RST0 | |
| [19] CAM_RST1 | AD27 | CAM_RST1 | |
| [19] CAM_PDN0 | AD29 | CAM_PDN0 | |
| [19] CAM_PDN1 | AC30 | CAM_PDN1 | |
| [19] CMMCLK | AC26 | CAM_CLK0 | |

### SPI

| | | | |
|---|---|---|---|
| [18] GPIO_CTP_RSTB | AJ1 | SPI_CSB | |
| [17] AUDIOPA_SD | | | |
| TP1202 TP-0.5MM | AL2 | SPI_CLK | |
| [22] EINT_SD | AH1 | SPI_MO | |
| [16] EINT_NFC | AJ2 | SPI_MI | |

### DPI

| | | | |
|---|---|---|---|
| DPI_D0 | W31 | | |
| DPI_D1 | W30 | | |
| DPI_D2 | V28 | | |
| DPI_D3 | V30 | | |
| DPI_D4 | Y27 | | |
| DPI_D5 | AA27 | | |
| DPI_D6 | AA30 | | |
| DPI_D7 | AB31 | | |
| DPI_D8 | AB30 | | |
| DPI_D9 | V29 | | |
| DPI_D10 | W28 | | |
| DPI_D11 | AB29 | | |
| DPI_DE | Y31 | | |
| DPI_CK | W29 | | |
| DPI_HSYNC | W27 | | |
| DPI_VSYNC | V26 | | |

### I2S

| | | | |
|---|---|---|---|
| [19] EINT_ALPS | V30 | I2S0_MCK | |
| [20] M_RESET | U30 | I2S0_BCK | |
| [16] GPIO_NFC_IRQ | T31 | I2S0_LRCK | |
| [6] EINT_MT6311 | U31 | I2S0_DI | |
| [22] URXD0 | V28 | I2S1_MCK | |
| [22] UTXD0 | V27 | I2S1_BCK | |
| TP1205 TP-0.5MM | U27 | I2S1_LRCK | |
| TP1206 TP-0.5MM | U26 | I2S1_DO | |
| [5] VOW_CLK_MISO | AB28 | VOW_CLK_MISO | |

MT6752/677PIN
MT6752V/L

U1001-D

## MT6752-SBS

### USB

| | | | |
|---|---|---|---|
| [21] USB_DP | T2 | USB_DP_P0 | |
| [21] USB_DM | T1 | USB_DM_P0 | |
| [5] USB_ID | AB4 | IDDIG | |
| [7] DRV_VBUS | AA1 | DRVBUS | |
| | P3 | USB_DP_P1 | |
| | R2 | USB_DM_P1 | |

5.1KR — R1201 +/-1% — USB_VRT_P0 — T4 — USB_VRT_P0

### BC

| | | | |
|---|---|---|---|
| | R4 | CHD_DP_P0 | |
| | R3 | CHD_DM_P0 | |
| [5] CHD_DP_P0 | | | |
| [5] CHD_DM_P0 | | | |

### KEYPAD

R1210 NC — AG3 KPROW1, AE3 KPROW0

| | | | |
|---|---|---|---|
| [21] GPIO_SUBID | AF2 | KPCOL1 | |
| [22] KCOL0 | AG2 | KPCOL0 | |

### I2C

VIO18_PMU — R1202 4.7KR, R1203 4.7KR

| | | | |
|---|---|---|---|
| [6,7,18] SCL0 | T30 | SCL0 | |
| [6,7,18] SDA0 | R30 | SDA0 | |
| VIO18_PMU — R1204 4.7KR, R1205 4.7KR | | | |
| | R28 | SCL1 | |
| | R29 | SDA1 | |
| [16,19,20] SCL1 | | | |
| [16,19,20] SDA1 | | | |
| | R26 | SCL2 | |
| | R27 | SDA2 | |
| | T27 | SCL3 | |
| | T28 | SDA3 | |
| [6] SCL2 | | | |
| [6] SDA2 | | | |

VIO18_PMU — R1208 4.7KR, R1209 4.7KR

| | | | |
|---|---|---|---|
| [19] SCL3 | | | |
| [19] SDA3 | | | |

### UART

### WCN 6625

| | | | |
|---|---|---|---|
| [15] GPS_RX_IP | G30 | GPS_RXIP | |
| [15] GPS_RX_IN | G31 | GPS_RXIN | |
| [15] GPS_RX_QP | F31 | GPS_RXQP | |
| [15] GPS_RX_QN | F30 | GPS_RXQN | |
| [15] F2W_CLK | P28 | F2W_CLK | |
| [15] F2W_DATA | P27 | F2W_DATA | |
| [15] WB_RX_IP | N31 | WB_RXIP | |
| [15] WB_RX_IN | M31 | WB_RXIN | |
| [15] WB_RX_QP | M30 | WB_RXQP | |
| [15] WB_RX_QN | L30 | WB_RXQN | |
| [15] WB_TX_IP | K30 | WB_TXIP | |
| [15] WB_TX_IN | K31 | WB_TXIN | |
| [15] WB_TX_QP | J31 | WB_TXQP | |
| [15] WB_TX_QN | J30 | WB_TXQN | |

MT6752/677PIN
MT6752V/L

### MSDCs

| | | | |
|---|---|---|---|
| MSDC0_RSTB | E28 | MSDC0_RSTB | [14] |
| MSDC0_CMD | B31 | MSDC0_CMD | [14] |
| MSDC0_CLK | A29 | MSDC0_CLK | [14] |
| MSDC0_DSL | A30 | MSDC0_DSL | [14] |
| MSDC0_DAT7 | D30 | MSDC0_DAT7 | [14] |
| MSDC0_DAT6 | B30 | MSDC0_DAT6 | [14] |
| MSDC0_DAT5 | C29 | MSDC0_DAT5 | [14] |
| MSDC0_DAT4 | D28 | MSDC0_DAT4 | [14] |
| MSDC0_DAT3 | C30 | MSDC0_DAT3 | [14] |
| MSDC0_DAT2 | D29 | MSDC0_DAT2 | [14] |
| MSDC0_DAT1 | B29 | MSDC0_DAT1 | [14] |
| MSDC0_DAT0 | B28 | MSDC0_DAT0 | [14] |
| MSDC1_CLK | G1 | MSDC1_CLK | [13] |
| MSDC1_CMD | H4 | MSDC1_CMD | [13] |
| MSDC1_DAT3 | G2 | MSDC1_DAT3 | [13] |
| MSDC1_DAT2 | H2 | MSDC1_DAT2 | [13] |
| MSDC1_DAT1 | G4 | MSDC1_DAT1 | [13] |
| MSDC1_DAT0 | H3 | MSDC1_DAT0 | [13] |

### CONN_IF

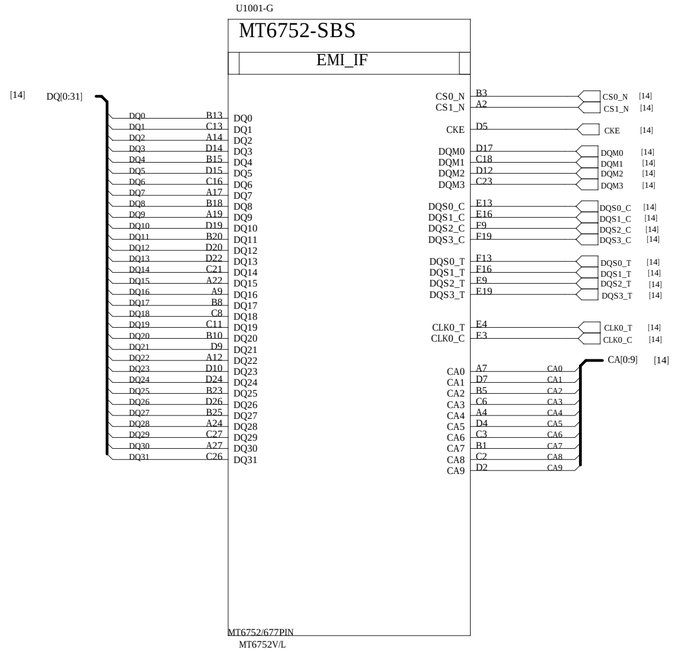
| | | | |
|---|---|---|---|
| WB_CTRL0 | J29 | WB_CTRL0 | [15] |
| WB_CTRL1 | J28 | WB_CTRL1 | [15] |
| WB_CTRL2 | K28 | WB_CTRL2 | [15] |
| WB_CTRL3 | L29 | WB_CTRL3 | [15] |
| WB_CTRL4 | L28 | WB_CTRL4 | [15] |
| WB_CTRL5 | M28 | WB_CTRL5 | [15] |
| WB_SCLK | L27 | CONN_SCLK | [15] |
| WB_SDATA | M27 | CONN_SDATA | [15] |
| WB_SEN | P30 | CONN_SEN | [15] |
| XIN_WBG | J26 | CONN_XO_IN | [15] |
| WB_RSTB | N30 | CONN_RSTB | [15] |

### PCM (ext MD)

### GPIO

| | | | |
|---|---|---|---|
| SRCLKENAI | AH3 SRCLKENAI | SRCLKENAI | [16] |
| PWM_A | AH2 EINT_CTP | EINT_CTP | [18] |

| | | | |
|---|---|---|---|
| INT_SIM1 | Y4 | EINT_CARD | [3,22] |
| INT_SIM2 | Y5 | EINT_CARD | [3,22] |


U1001-G
MT6752-SBS
EMI_IF
[14] DQ[0:31]
DQ0 B13 DQ0
DQ1 C13 DQ1
DQ2 A14 DQ2
DQ3 D14 DQ3
DQ4 B15 DQ4
DQ5 D15 DQ5
DQ6 C16 DQ6
DQ7 A17 DQ7
DQ8 B18 DQ8
DQ9 A19 DQ9
DQ10 D19 DQ10
DQ11 B20 DQ11
DQ12 D20 DQ12
DQ13 D22 DQ13
DQ14 C21 DQ14
DQ15 A22 DQ15
DQ16 A9 DQ16
DQ17 B8 DQ17
DQ18 C8 DQ18
DQ19 C11 DQ19
DQ20 B10 DQ20
DQ21 D9 DQ21
DQ22 A12 DQ22
DQ23 D10 DQ23
DQ24 D24 DQ24
DQ25 B23 DQ25
DQ26 D26 DQ26
DQ27 B25 DQ27
DQ28 A24 DQ28
DQ29 C27 DQ29
DQ30 A27 DQ30
DQ31 C26 DQ31
CS0_N B3 CS0_N [14]
CS1_N A2 CS1_N [14]
CKE D5 CKE [14]
DQM0 D17 DQM0 [14]
DQM1 C18 DQM1 [14]
DQM2 D12 DQM2 [14]
DQM3 C23 DQM3 [14]
DQS0_C E13 DQS0_C [14]
DQS1_C E16 DQS1_C [14]
DQS2_C F9 DQS2_C [14]
DQS3_C F19 DQS3_C [14]
DQS0_T F13 DQS0_T [14]
DQS1_T F16 DQS1_T [14]
DQS2_T E9 DQS2_T [14]
DQS3_T F19 DQS3_T [14]
CLK0_T E4 CLK0_T [14]
CLK0_C F3 CLK0_C [14]
CA[0:9] [14]
CA0 A7 CA0
CA1 D7 CA1
CA2 B5 CA2
CA3 C6 CA3
CA4 A4 CA4
CA5 D4 CA5
CA6 C3 CA6
CA7 B1 CA7
CA8 C2 CA8
CA9 D2 CA9
MT6752/677PIN
MT6752V/L

Schematic design notice of "20_POWER_MT6325" page.

Note 20-1: PAD_PWRAP_SPI0_MI and PAD_PWRAP_SPI0_MO are DRAM feature in bootstrap.

Note: 20-1

UVLO_VTH R RANGE:
200KOHM ~ 250KOHM

8 Core DVFS FB setting (8 Core and 4 Core Co-Layout)

| | |
|---|---|
| VGP1 | CTP |
| VGP2 | MHL |
| VGP3 | Sub-Cam |

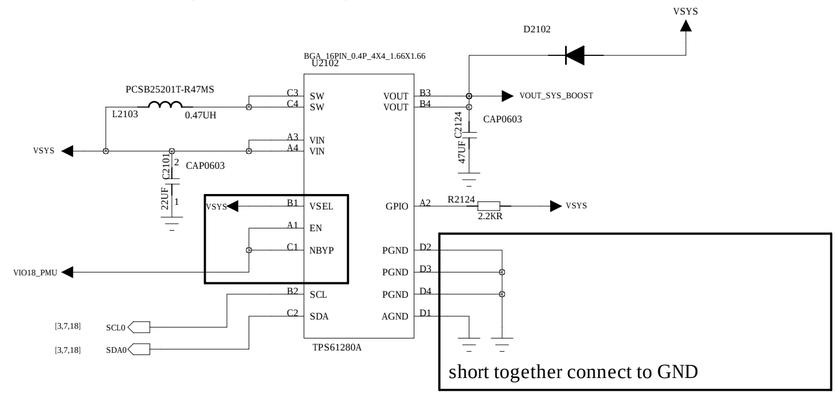
The Layout constraint requires sufficient bypass cap. LDO will not have stability problems

Audio

AU_REFN need single via to GND plane directly

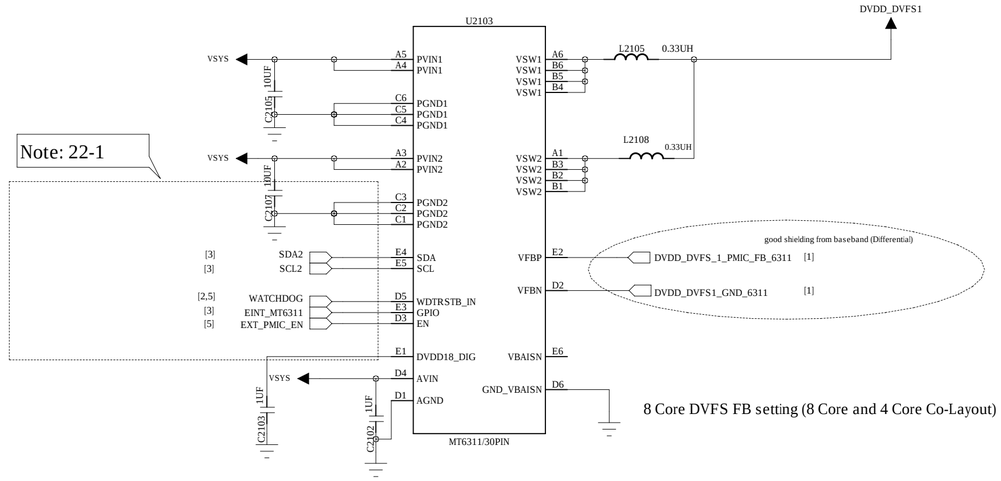
## Companion buck for VBAT@LV

TPS61280 I2C address: 0X75 (Write:0xEA, Read:0xEB)




## 2-Phase Buck

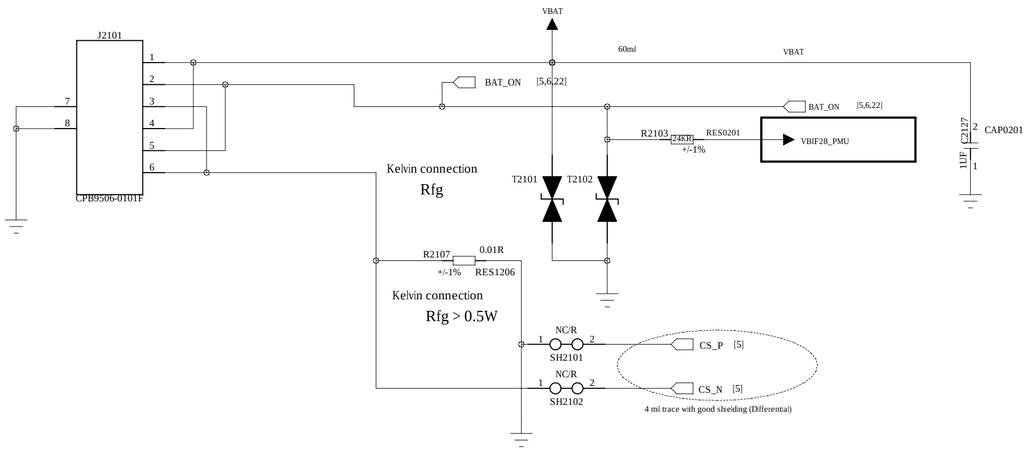
MT6311 / 2-Phase Buck I2C address: 0X6B (Write:0x, Read:0x)




Schematic design notice of "22_POWER_MT6311" page.

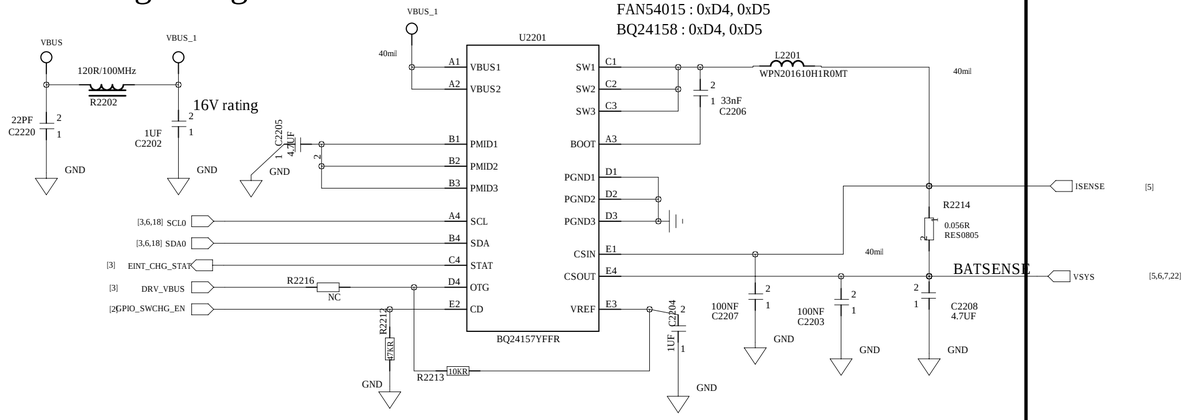
Note 22-1: MT6311 => Buck EN controlled by EXT_PMIC_EN from MT6325 and I2C.

## BATTERY CONNECTOR

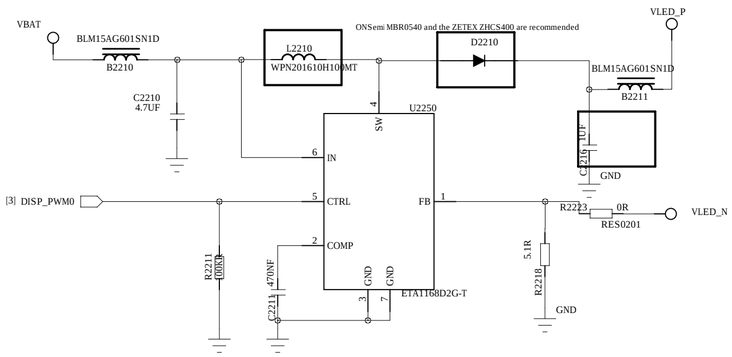


# Switching Charger

I2C Address
FN5405 : 0xD4, 0xD5
FAN54015 : 0xD4, 0xD5
BQ24158 : 0xD4, 0xD5

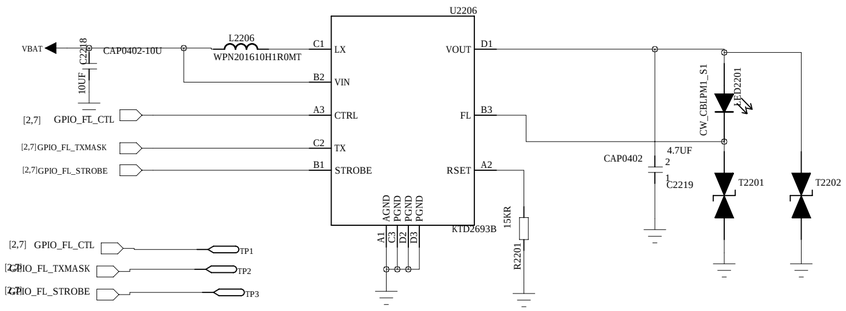


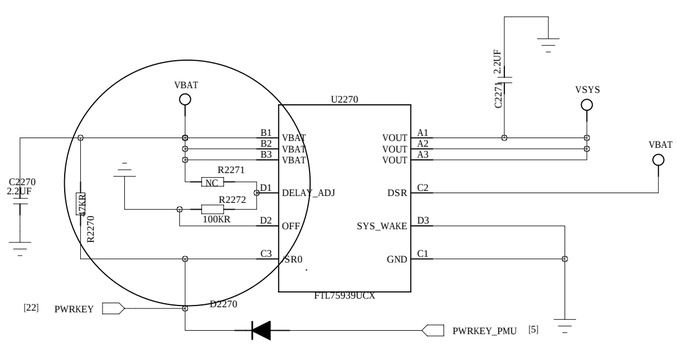

# LCM Backlight LED Driver



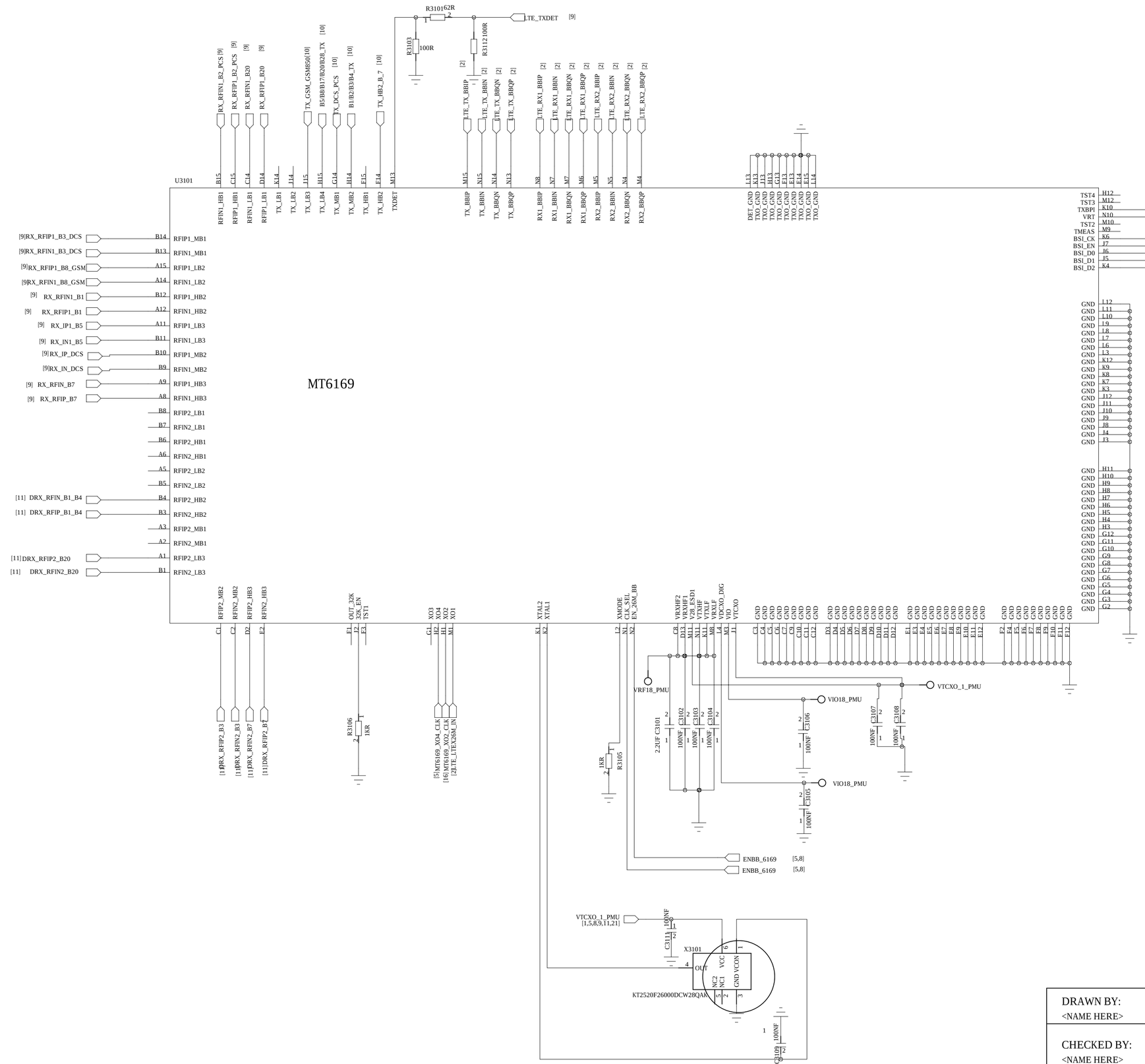

# Flash LED 5V Boost

Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)




boost£¿£¿£¿

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| CHECKED BY: <NAME HERE> | SIZE: A2 / DRAWING NO: <DRAWN NO HERE> / REV: <NO> | |
| | SHEET: No of No | <DATE HERE> |

# B7 TRX (EU only)

U3203
ECT818000157
L3202 2.7NHNC
C3201 22PF
U3202 CP1608-24R0822
C3228 18PFNC
C3203 18PF
R3201 51R
LTE_TXDET [8]
VTCXO_1_PMU
C3204 10PF
VMIPI_PMU
C3205 10PF
[2,10] LTE_MIPI0_SDATA
LTE_TRX_B7 [9]
LTE_TRX_B20 [9]
LTE_MIPI0_SCLK [2,10]
LTE_TRX_B7
LTE_TRX_B20
B5_PA_OUT [10]
B8_PA_OUT [10]
LB_PA_OUT [10]
HB_PA_OUT [10]
B1_PA_OUT [10]
B2_PA_OUT [10]
B34_PA_OUT [10]
B20/B17_PA_OUT [10]
TX_B7_PA_OUT [10]
TRX2
BAND5_TX
BAND8_TX
GSM_LB_TX
GSM_HB_TX
TRX1
BAND1_TX
BAND2_TX
BAND4_TX
GND
TRX3
ANT
VDD
VIO
SDATA
TRX4
SCLK
DCS_RX
BAND8_RX
BAND2_RX
BAND1_RX
BAND4_RX
U3201
MSW6SGNEF70
L3203 3.9NH
C3206 3.9PF
NC L3206 4.3NH
C3207 3.9PF
RX_RFIP1_B2_PCS [8]
RX_RFIN1_B2_PCS [8]
L3207 8.2NH
C3209 5.1NH
L3208 4.3NHNC
C3210 5.1NH
RX_RFIP1_B8_GSM [8]
RX_RFIN1_B8_GSM [8]
L3210 4.3NH
C3215 15PF
L3211 4.3NHNC
C3214 15PF
RX_RFIP1_B3_DCS [8]
RX_RFIN1_B3_DCS [8]
L3212NC 5.6NH
C3224 1.0NH
L3219 2.2NH
U3204 D6HN2G655BN54
Delete U1630 on 6/21
L3220 5.6NH
C3225 1PF1
L3222 18PF
NC
C3226 1PF
RX_RFIN_B7 [8]
RX_RFIP_B7 [2,10] [8]
C3227 18PF
L3224 NC3.3NH
L3209 2.2NHNC
C3211 18PF
U3206 TFSL06050915-4108B1
U3205
SAYFH806MCA0F0A
L3205 10NH
R3202 0R
C3208 10NH
L3204 10NH
L3201 10NHNC
C3202 10NH
RX_RFIN1_B20 [8]
RX_RFIP1_B20 [8]
R3303
R3204
L3221 NC10NH
C3221 5.1NH
C3222 5.1NH
L3223 10NH
C3218 5.1NH
L3215 10NH
C3216 10NHNC
C3219 5.1NH
RX_IP1_B5 [8]
RX_IN1_B5 [8]
RX_IP_DCS [8]
RX_IN_DCS [8]
C3217 4.7PF
L3213 2.7NH
L3214 2.7NHNC
C3216 4.7PF
RX_RFIN1_B1 [8]
RX_RFIP1_B1 [8]

| | | |
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| DRAWN BY: <NAME HERE> | MODULE <MODULE NAME HERE> | TITLE: <TITLE NAME HERE> |
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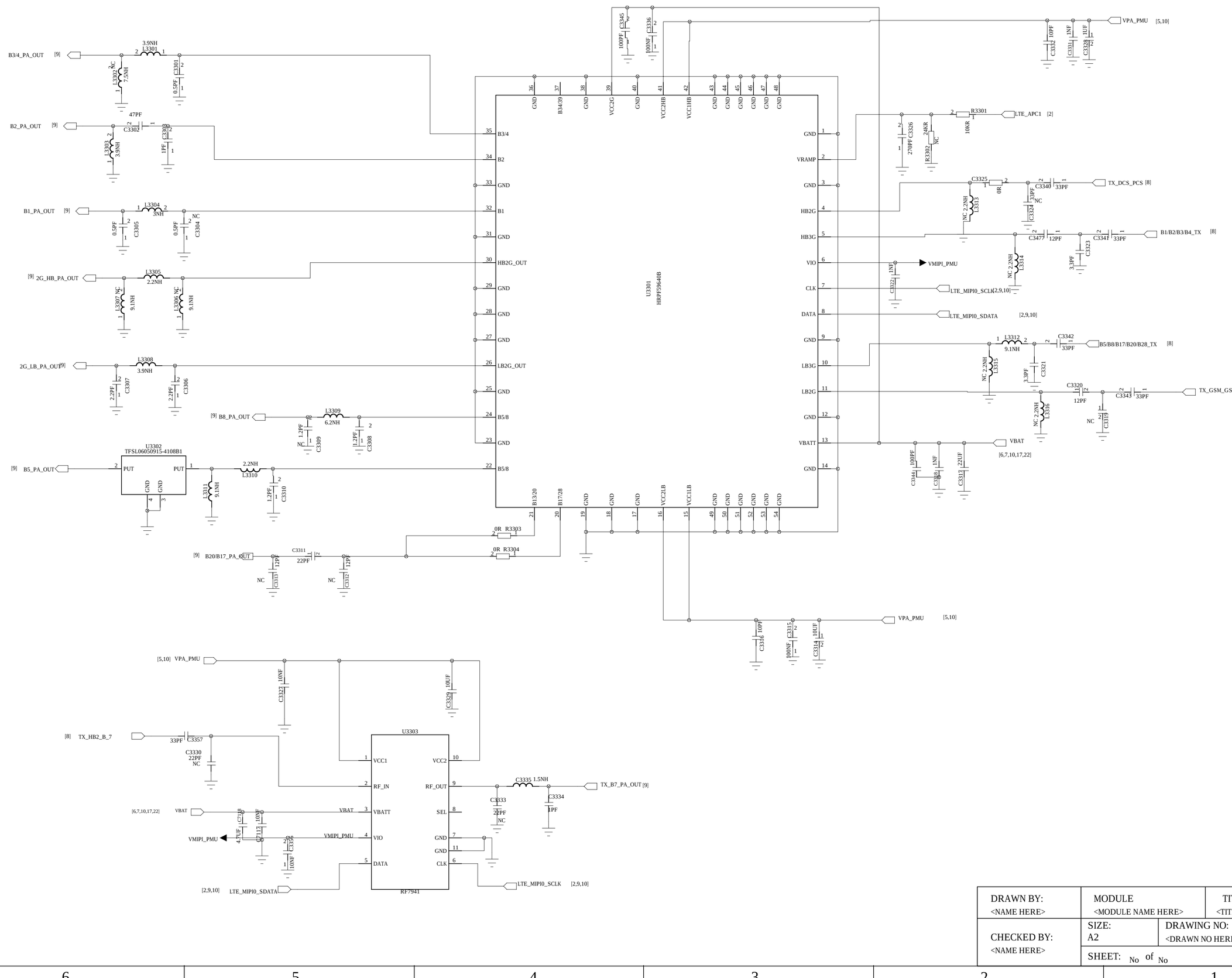
| | SHEET: No of No | <DATE HERE> |

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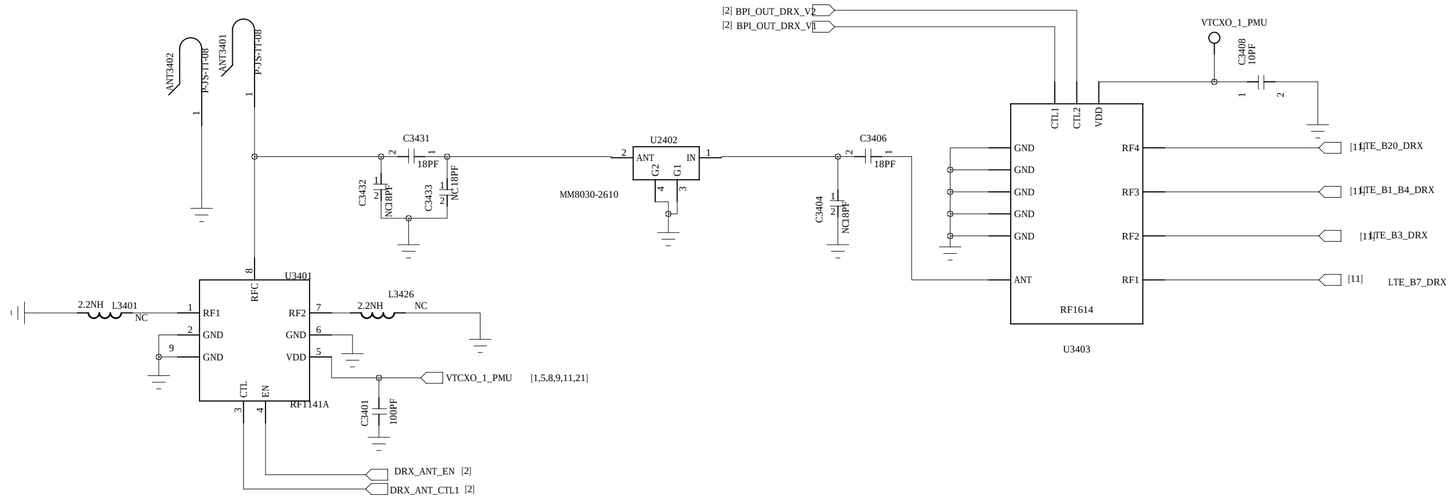
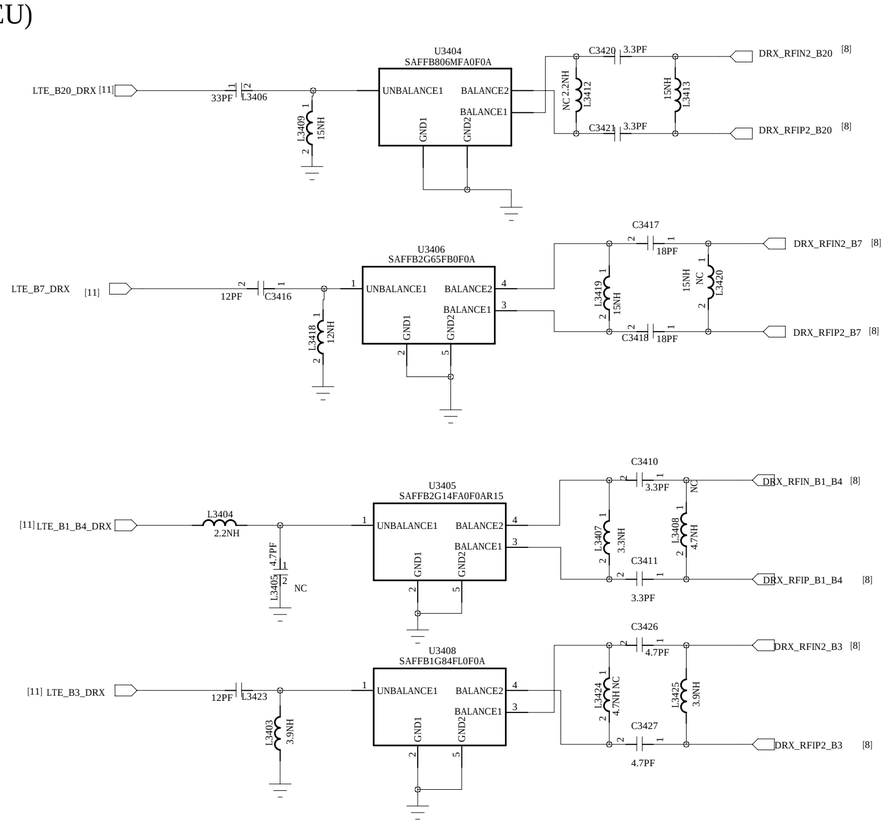



B20 DRX(EU)

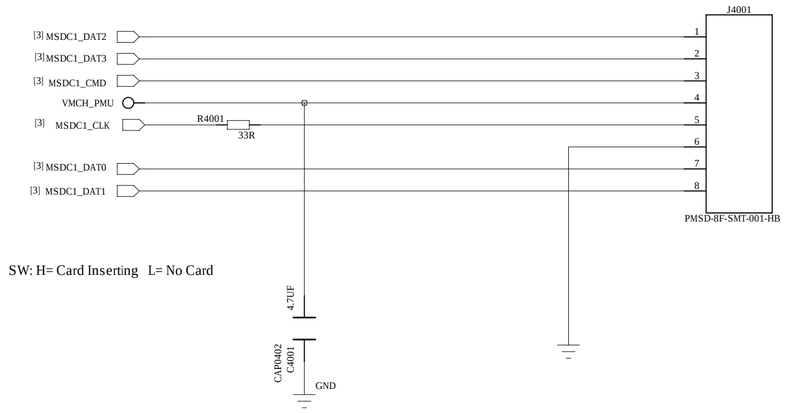



B1/4 DRX (EU & LATAM)

B3 DRX(EU)
B2 DRX(LATAM)

| | | | |
|---|---|---|---|
| DRAWN BY: <NAME HERE> | MODULE <MODULE NAME HERE> | TITLE: <TITLE NAME HERE> | |
| CHECKED BY: <NAME HERE> | SIZE: A2 | DRAWING NO: <DRAWN NO HERE> | REV: <NO> |
| | SHEET: No of No | <DATE HERE> | |

# TFlash card



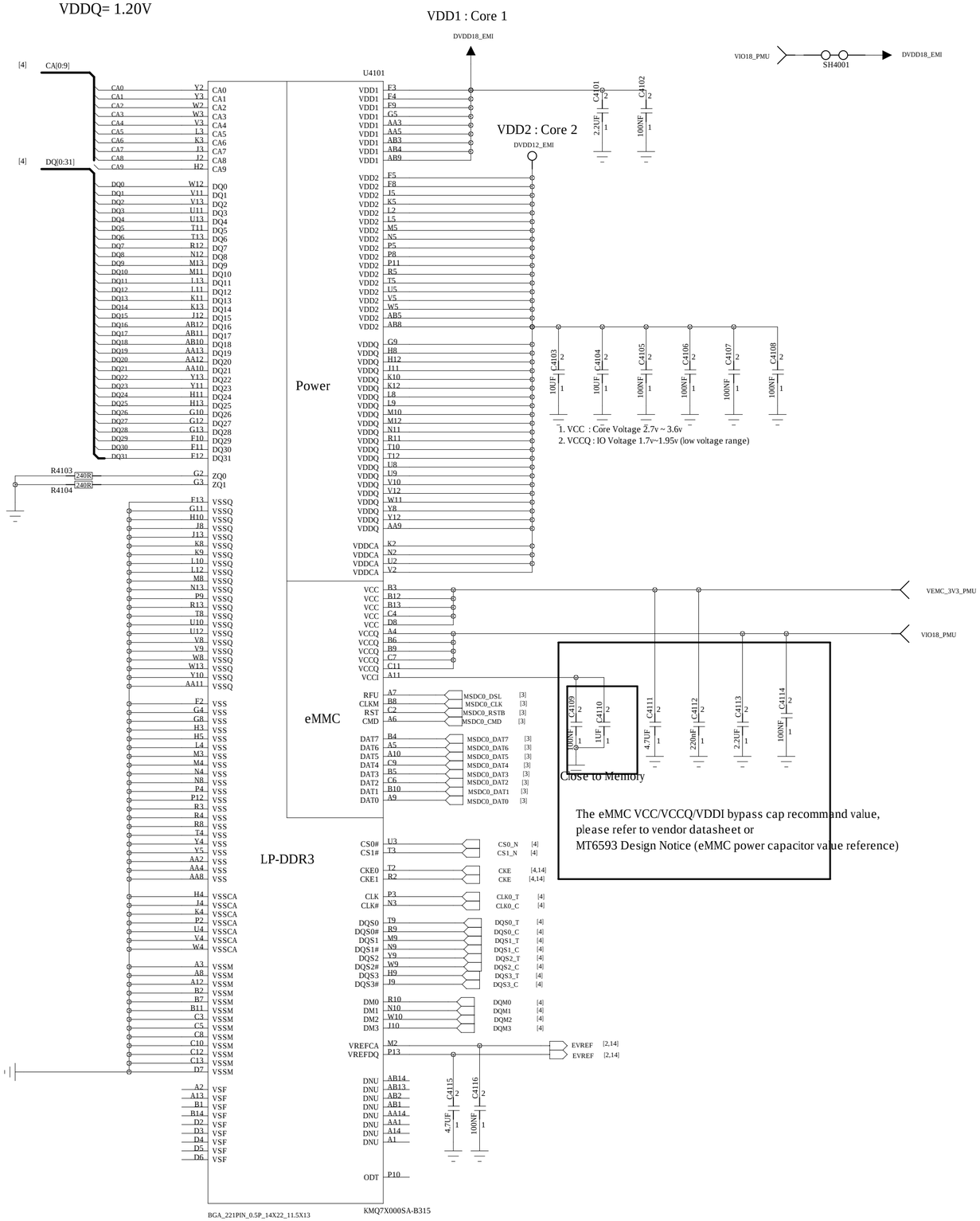

Schematic design notice of "41_MEMORY_SD Card" page.

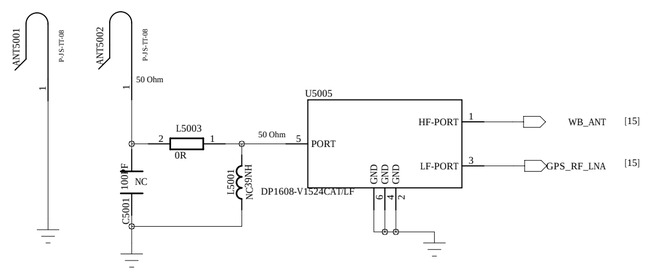
Note 41-1: The equivalent capacitance of ESD protection device must be <=0.5pF
-- otherwise it will result in NFC card mode function fail.

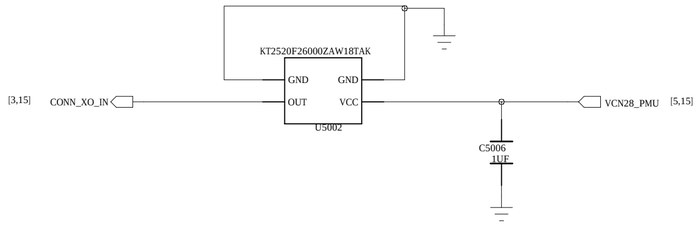
# eMMC+LPDDR3　　16GB eMMC + 16Gb LPDDR3

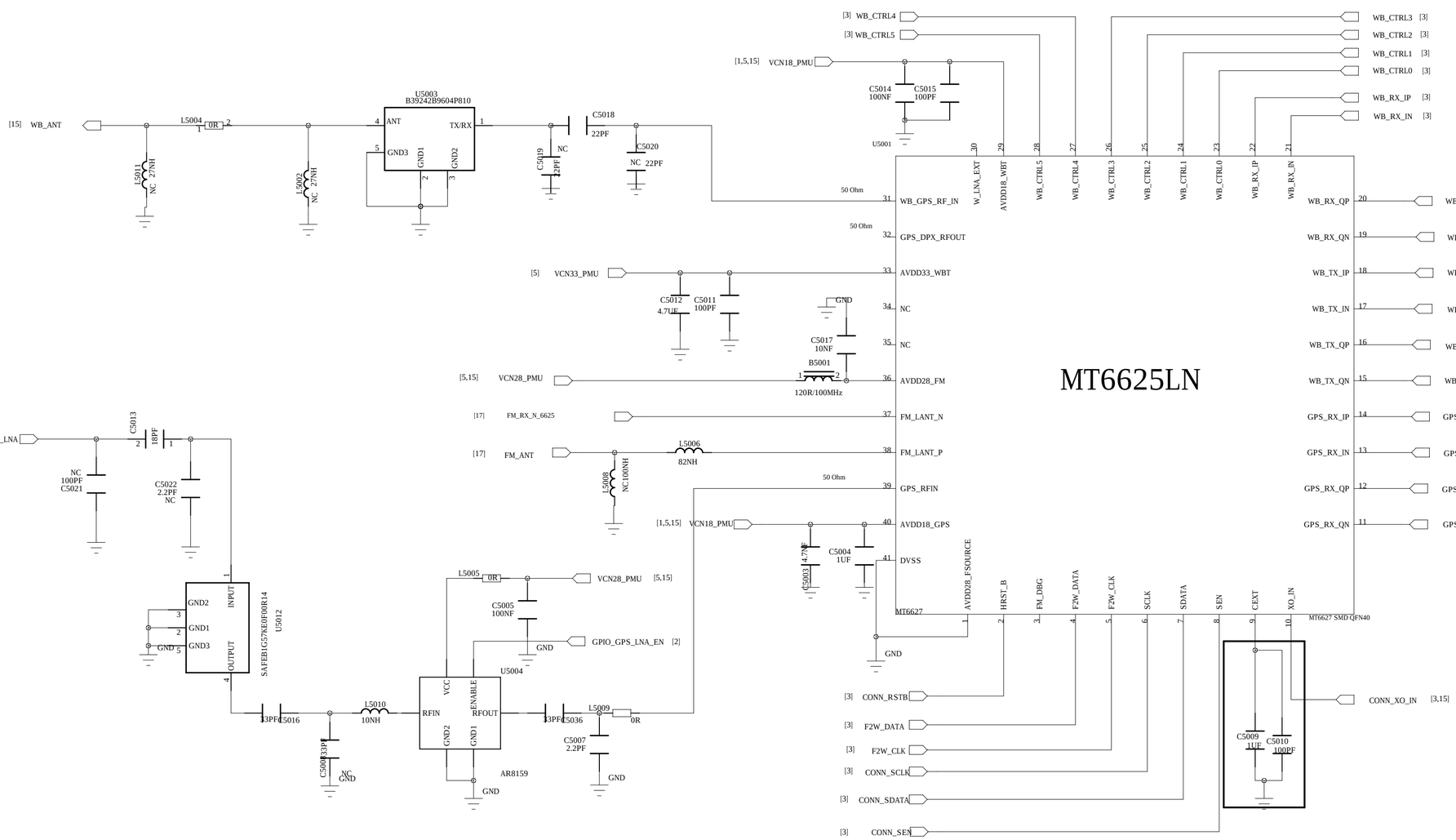
221 Ball, 0.5mm pitch

VDD1=1.8V
VDD2=1.20V
VDDCA=1.2V
VDDQ= 1.20V






# MT6625LN

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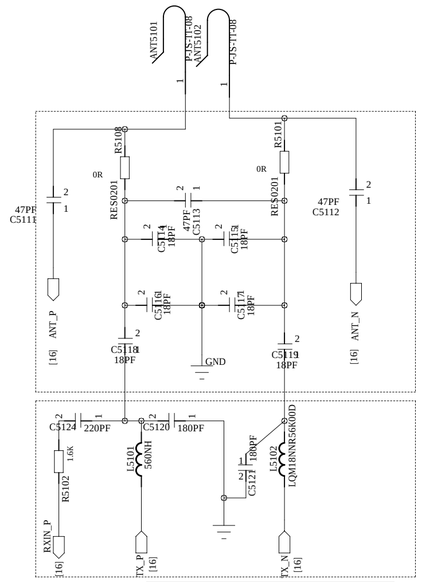
| | SHEET: No of No | <DATE HERE> | |

# NFC MT6605



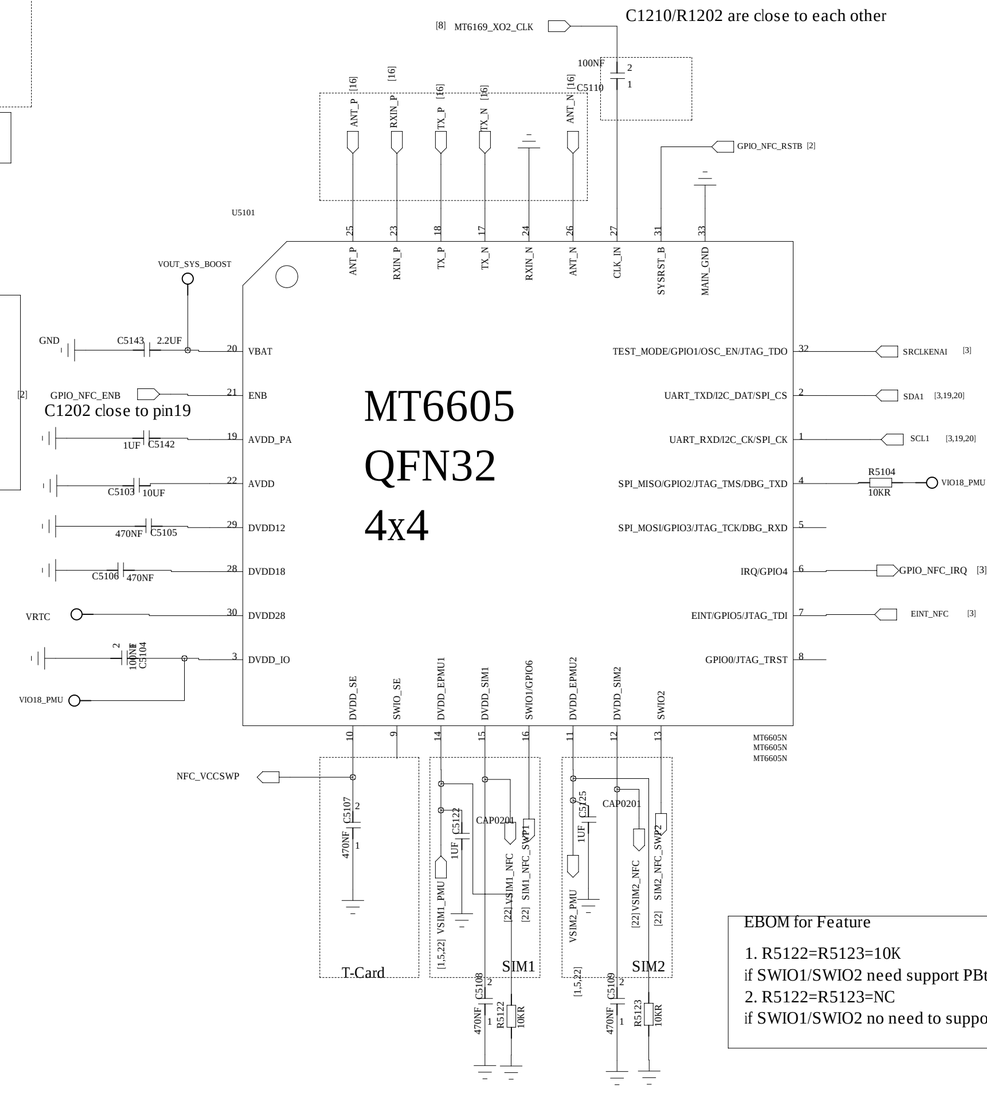

Components in this region
use 5% accuracy

C1211,C1212,C1213,C1214,C1215,C1216,C1217, C1218,
C1219 need to use 2% accuracy and 50V tolerance capacitor,
PS: 0201 cap can't tolerance 50V

POWER MODE[1:0]=[NFC_RST:NFC_VENB]

| Power Mode | NFC_RST | NFC_VENB |
|---|---|---|
| NFC enable (configure, R/W, card, polling loop, polling loop card listening) | 1 | 0 |
| NFC disable (HPD) | 0 | 1 |
| Hign battery card listening | 1 | 1 |
| Reset | 0 | 0 |

C1210/R1202 are close to each other




ENB (NFC_VEN)
1.Input pin
2.Internal pull low
3.Low active
4.If default NFC
would like to disable,
please configure to high

SYSRST_B (NFC_RST)
1.Input pin
2.Internal pull high
3.Low active

1.NFC_OSC_EN is output pin, and high active.
2.Need to connect to host SRCLKENAI and
SRCLKENAI pin need to be default low.

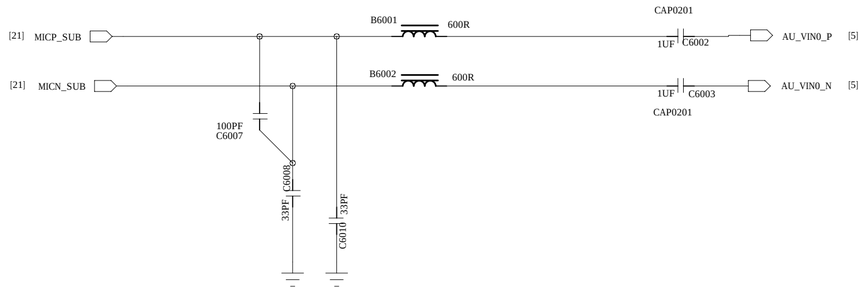
Only can use HW I2C.
SW I2C is not allowed. Address:0x28

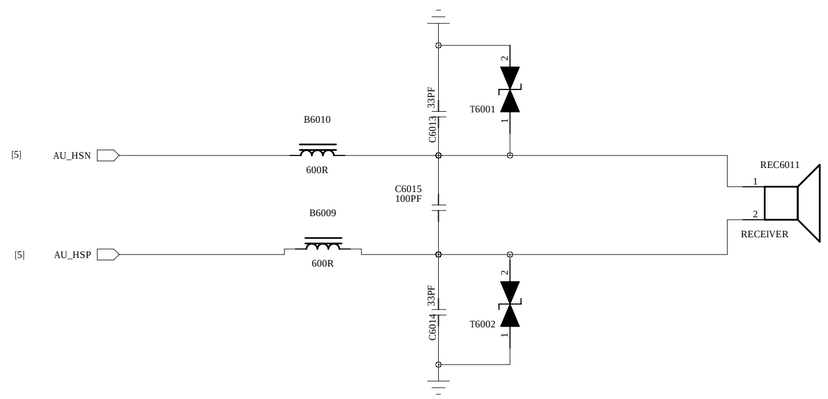
R1206 NC : XTAL MODE
R1206 10K : Co-Clock

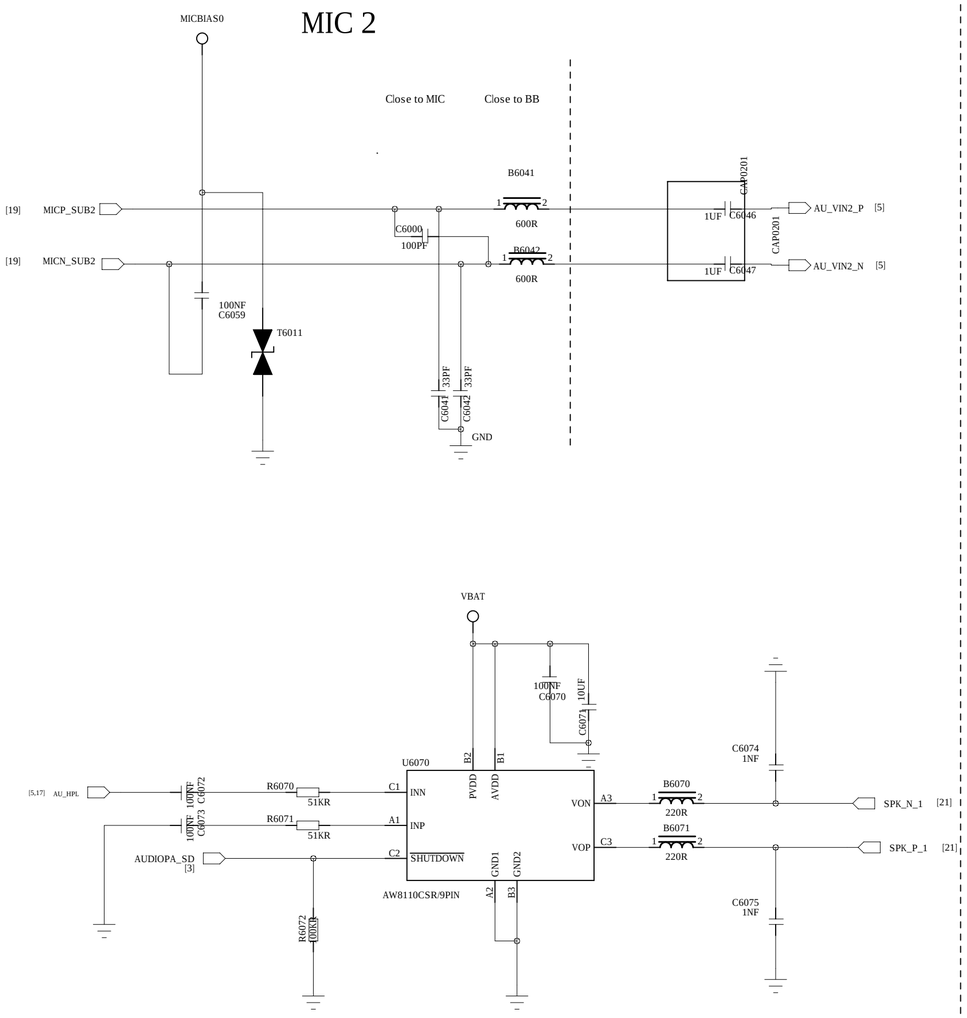
1.IRQ_NFC is output pin, and high active.
2.IRQ_NFC is also strap pin and host I/F
connected with IRQ need to be default low.

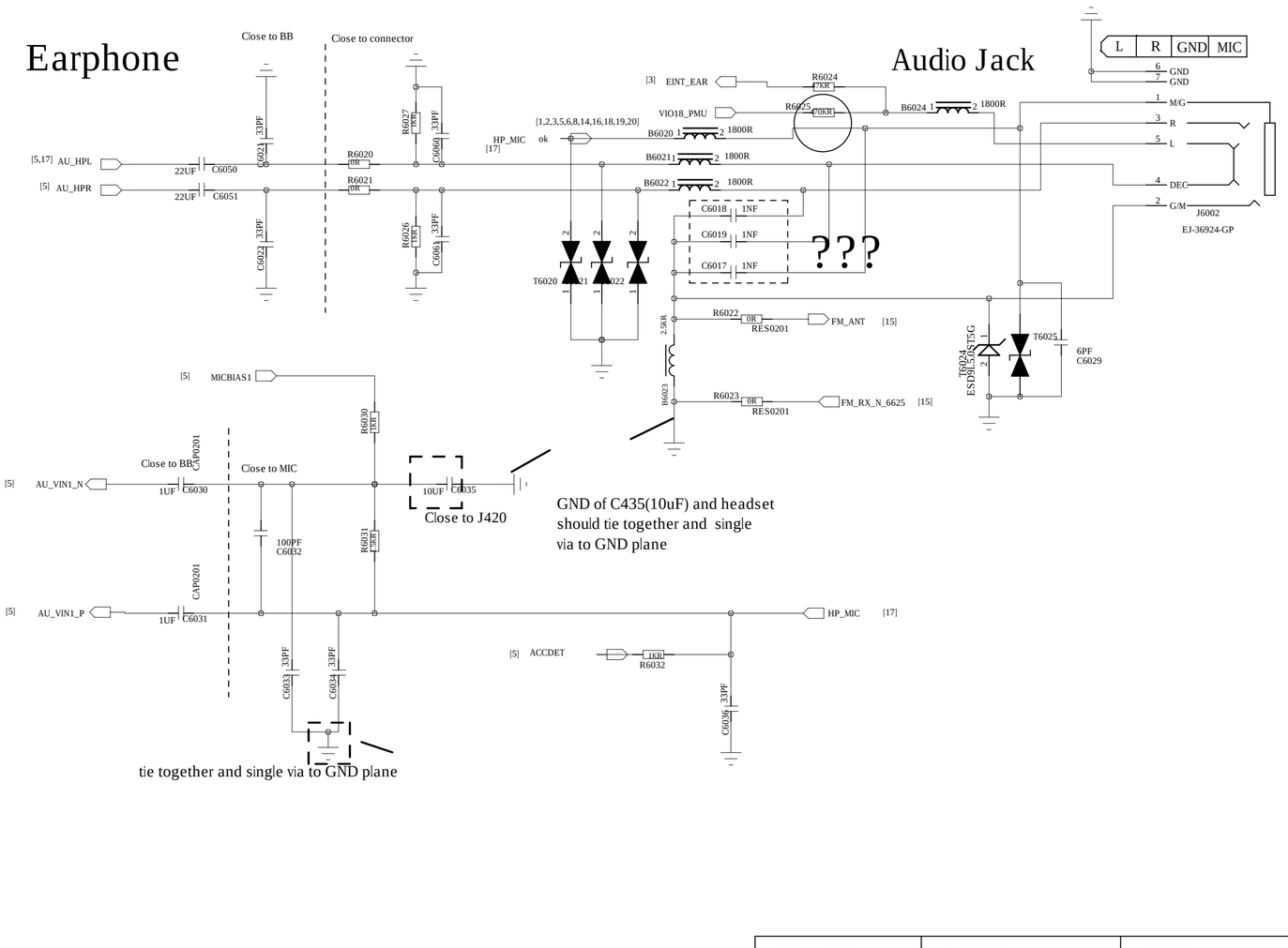
EBOM for Feature

1. R5122=R5123=10K
if SWIO1/SWIO2 need support PBtF
2. R5122=R5123=NC
if SWIO1/SWIO2 no need to support PBtF



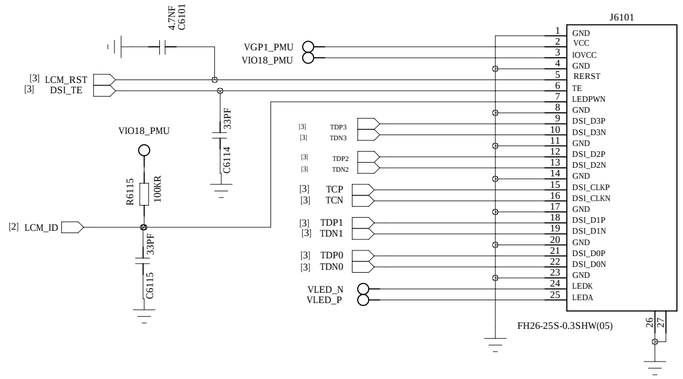



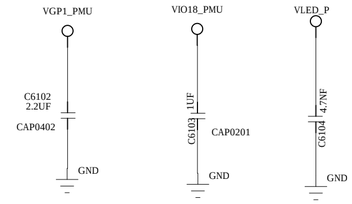




| | | | |
|---|---|---|---|
| DRAWN BY: <NAME HERE> | MODULE <MODULE NAME HERE> | TITLE: <TITLE NAME HERE> | |
| CHECKED BY: <NAME HERE> | SIZE: A2 | DRAWING NO: <DRAWN NO HERE> | REV: <NO> |
| | SHEET: No of No | | <DATE HERE> |

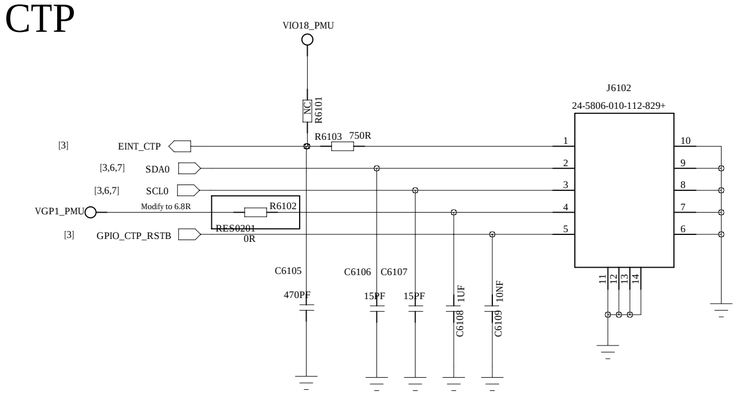
Archive

# LCM



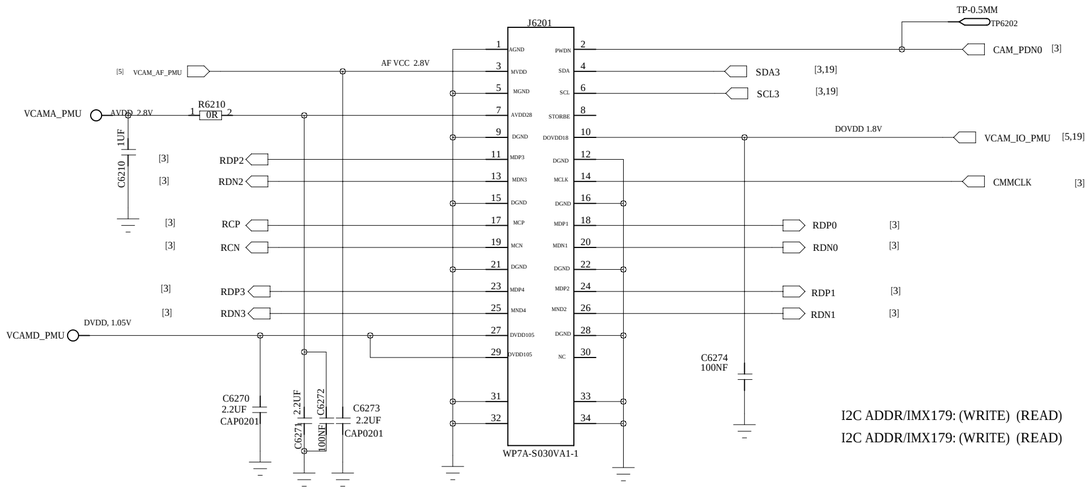




# CTP




GT917S's INT pin  CANNOT be pulled-up.

# Main Camera




I2C address:(write:0X20 ;read:0X21 )

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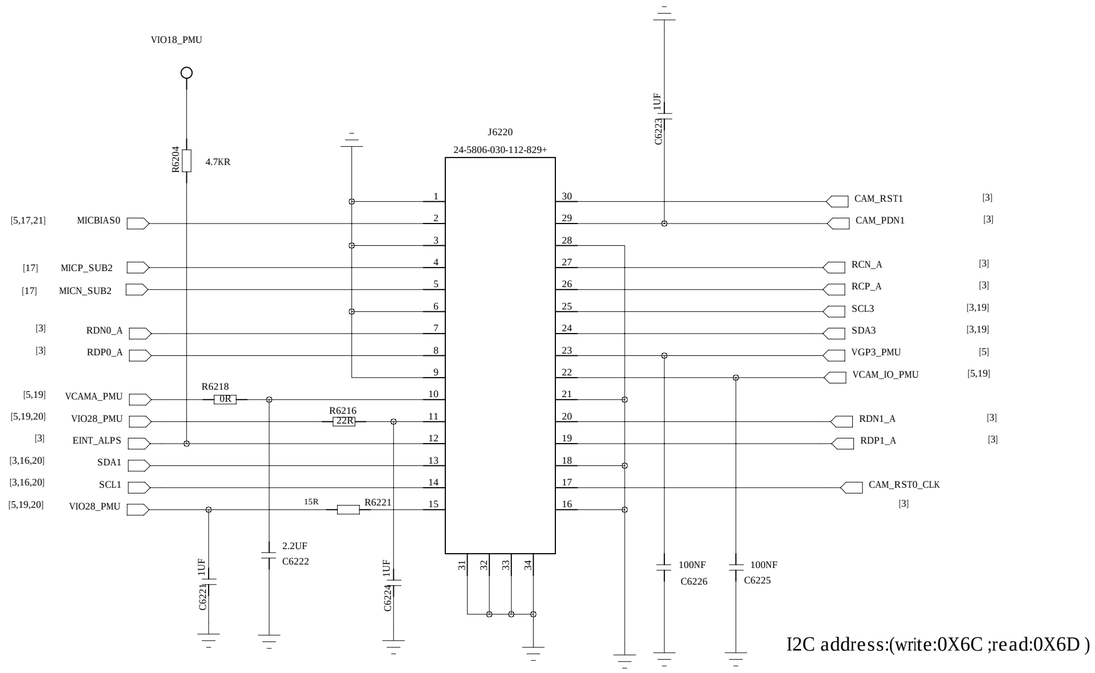
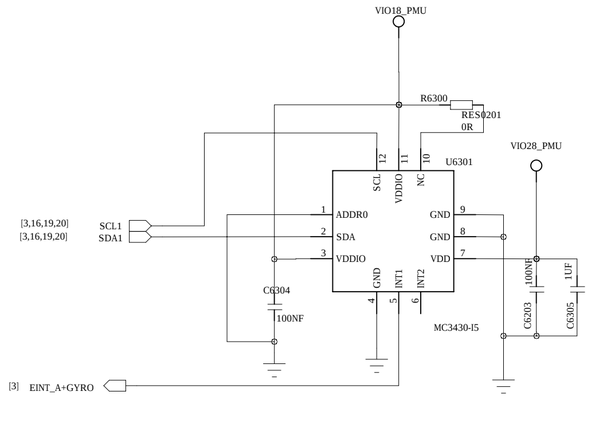
SUB CAM/PS/ALS CON



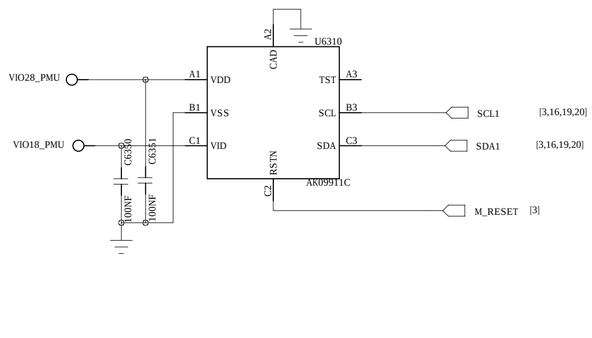

I2C address:(write:0X6C ;read:0X6D )

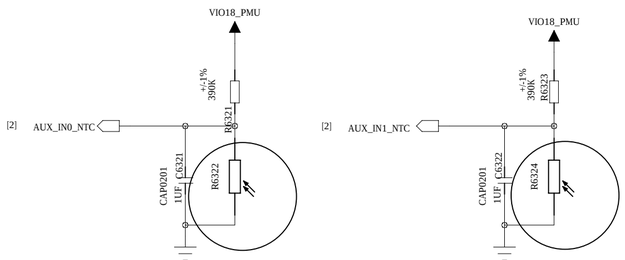
# G SENSOR



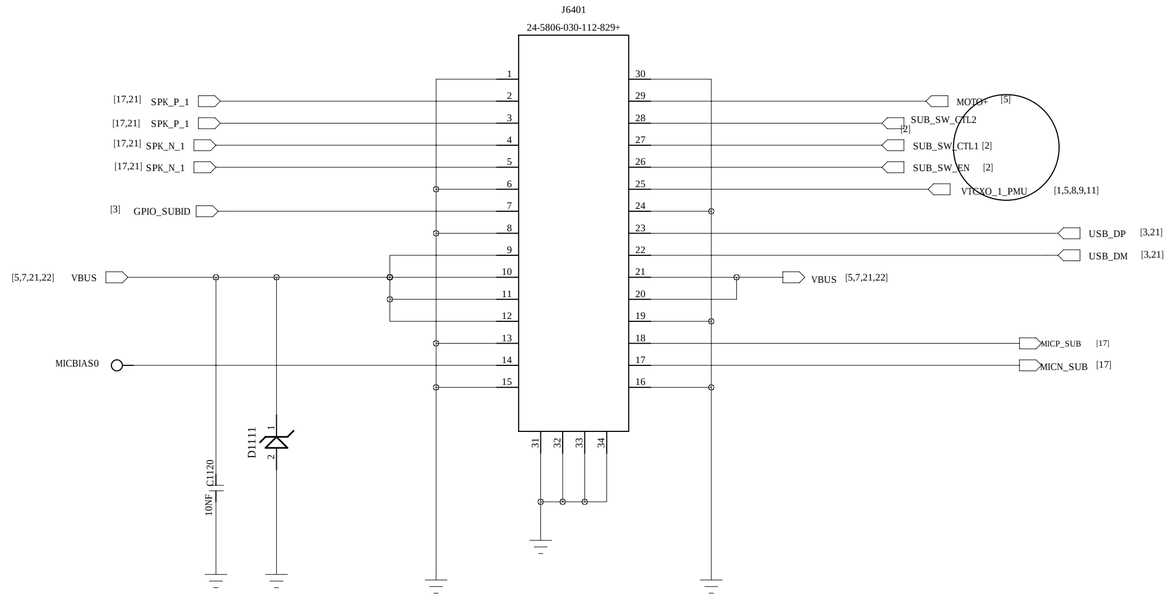

# M-SENSOR

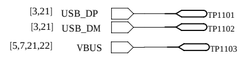
I2C address:0x0C(write:0x18;read:0x19)



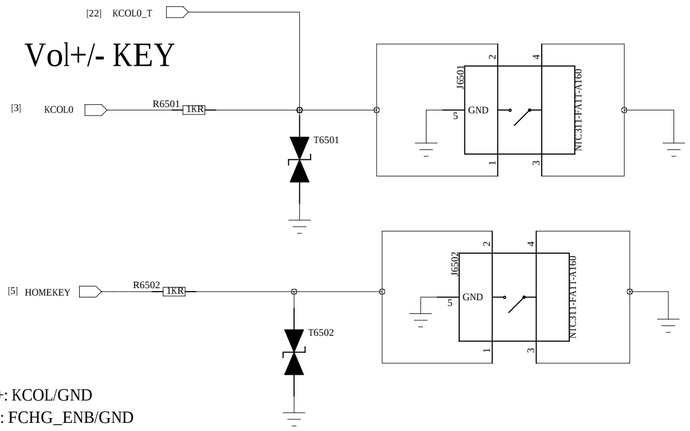



# Sub board IO


J6401
24-5806-030-112-829+
[17,21] SPK_P_1
[17,21] SPK_P_1
[17,21] SPK_N_1
[17,21] SPK_N_1
[3] GPIO_SUBID
[5,7,21,22] VBUS
MICBIAS0
D1111
C1120
10NF
MOTO+ [5]
SUB_SW_CTL2 [2]
SUB_SW_CTL1 [2]
SUB_SW_EN [2]
VTSYO_1_PMU [1,5,8,9,11]
USB_DP [3,21]
USB_DM [3,21]
VBUS [5,7,21,22]
MICP_SUB [17]
MICN_SUB [17]

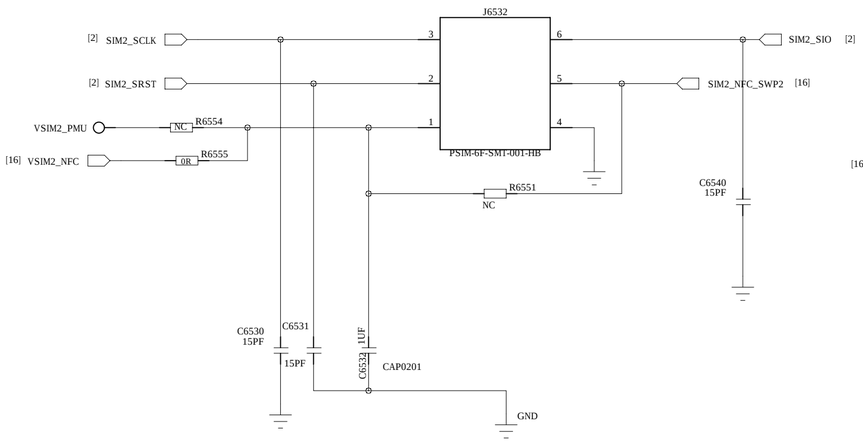

[3,21] USB_DP
[3,21] USB_DM
[5,7,21,22] VBUS
TP1101
TP1102
TP1103

# Vol+/- KEY



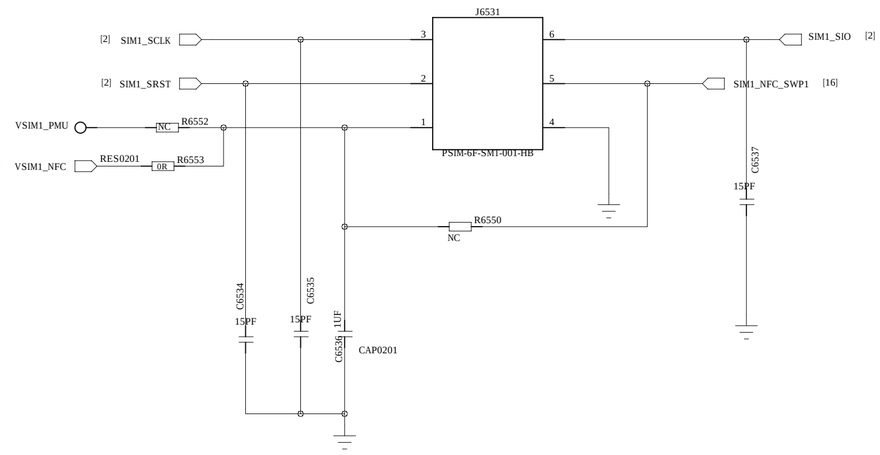

Vol+: KCOL/GND
Vol-: FCHG_ENB/GND

# SIM2 Card




DET: L=NO SIM; H= INSERT CARD

# SIM1 Card




DET: H=NO SIM; L= INSERT CARD

# Power KEY