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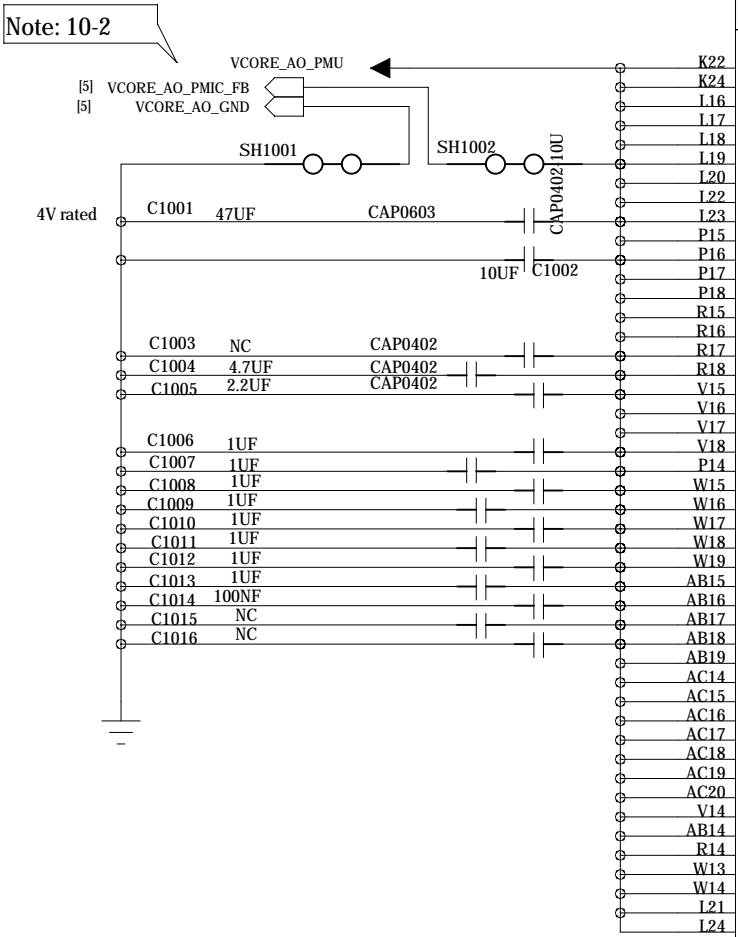
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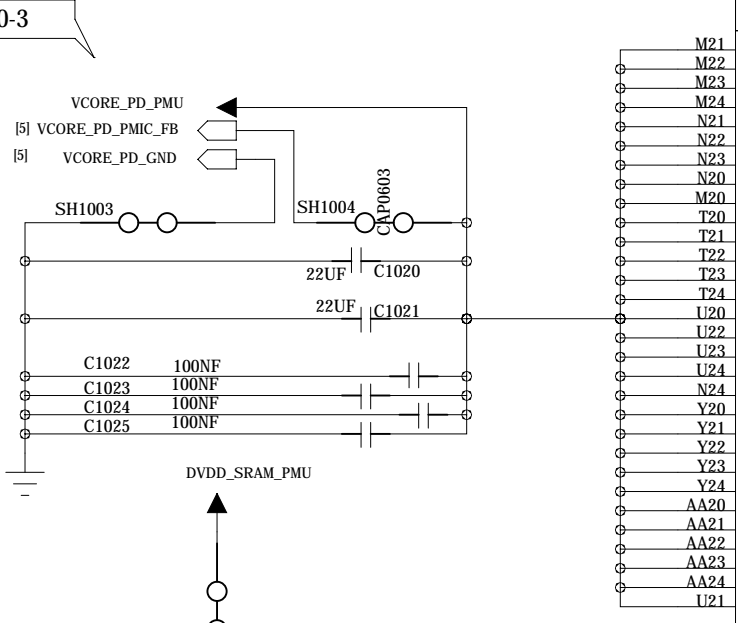
UT001-E

MT6752-SBS

VCCCK



VCCCK2



SRAM

VDDQ

GND

GND

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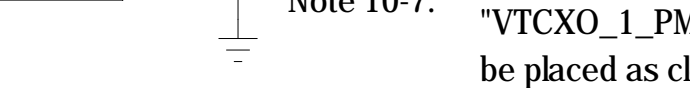
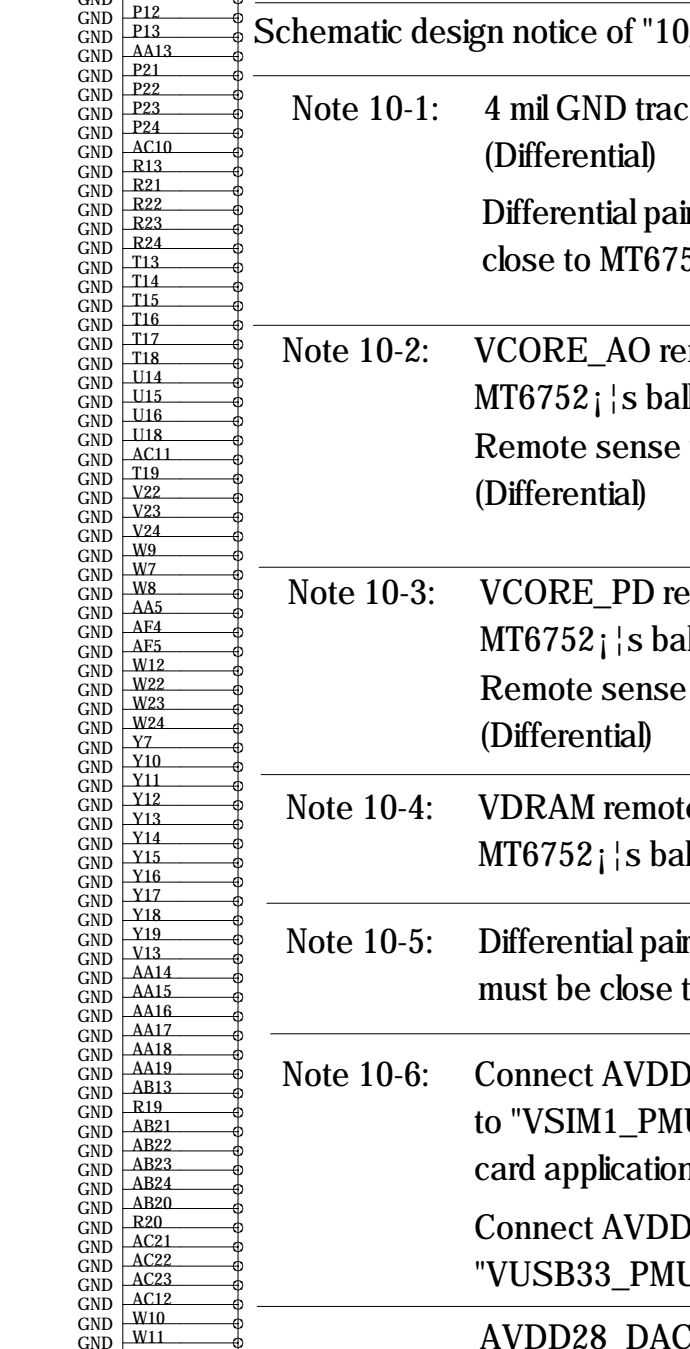
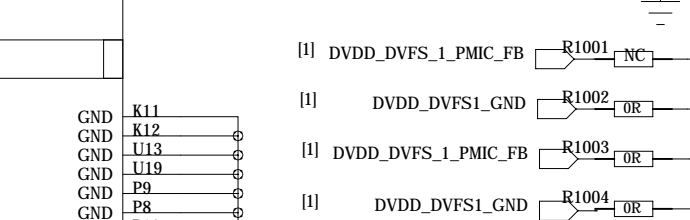
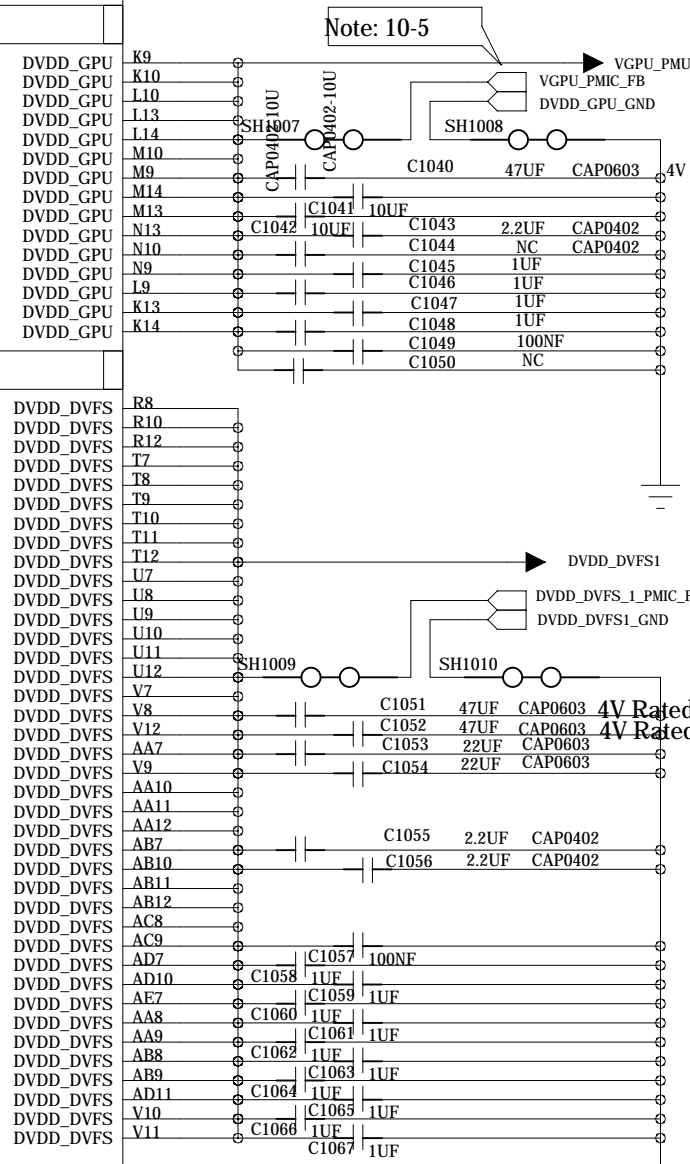
GND

GND

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GND

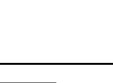
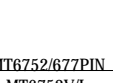
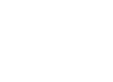
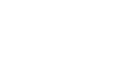
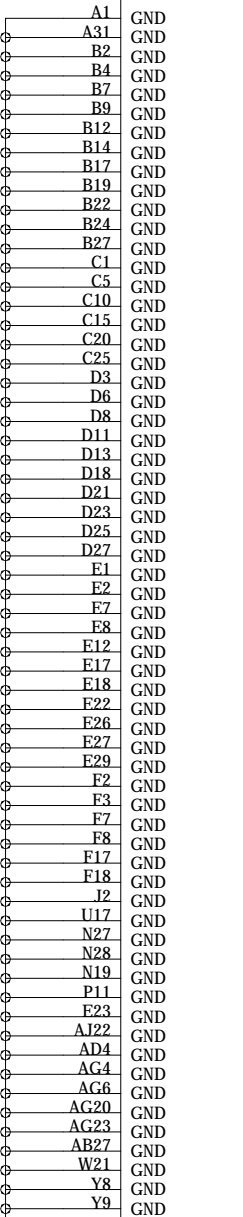
GND



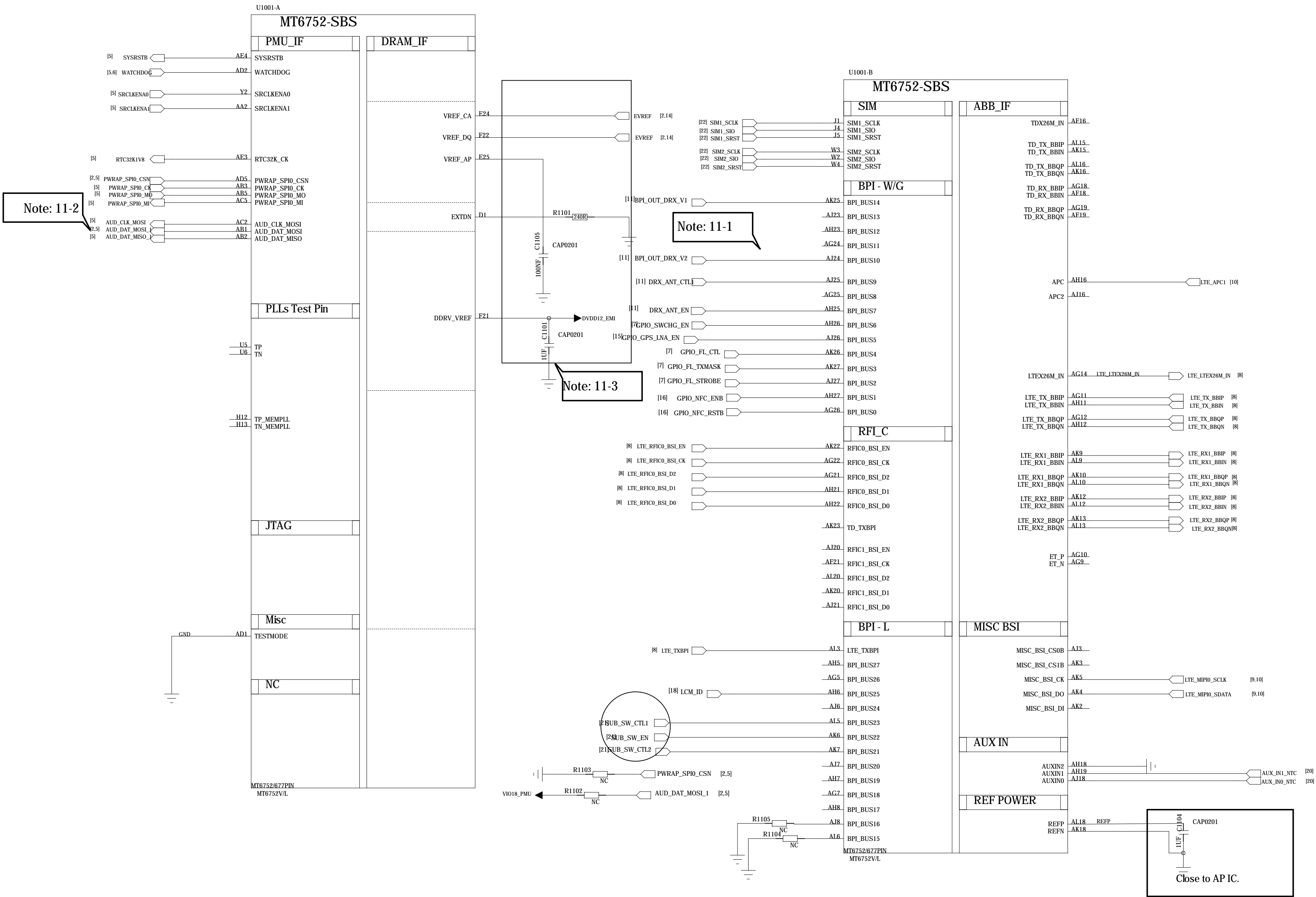
U1001-F

MT6752-SBS

GND



DRAWN BY: <NAME HERE>	MODULE <MODULE NAME HERE>	TITLE: <TITLE NAME HERE>
CHECKED BY: <NAME HERE>	SIZE: A2	DRAWING NO: <DRAWN NO HERE>
	SHEET: No of No	REV: <NO>
		<DATE HERE>



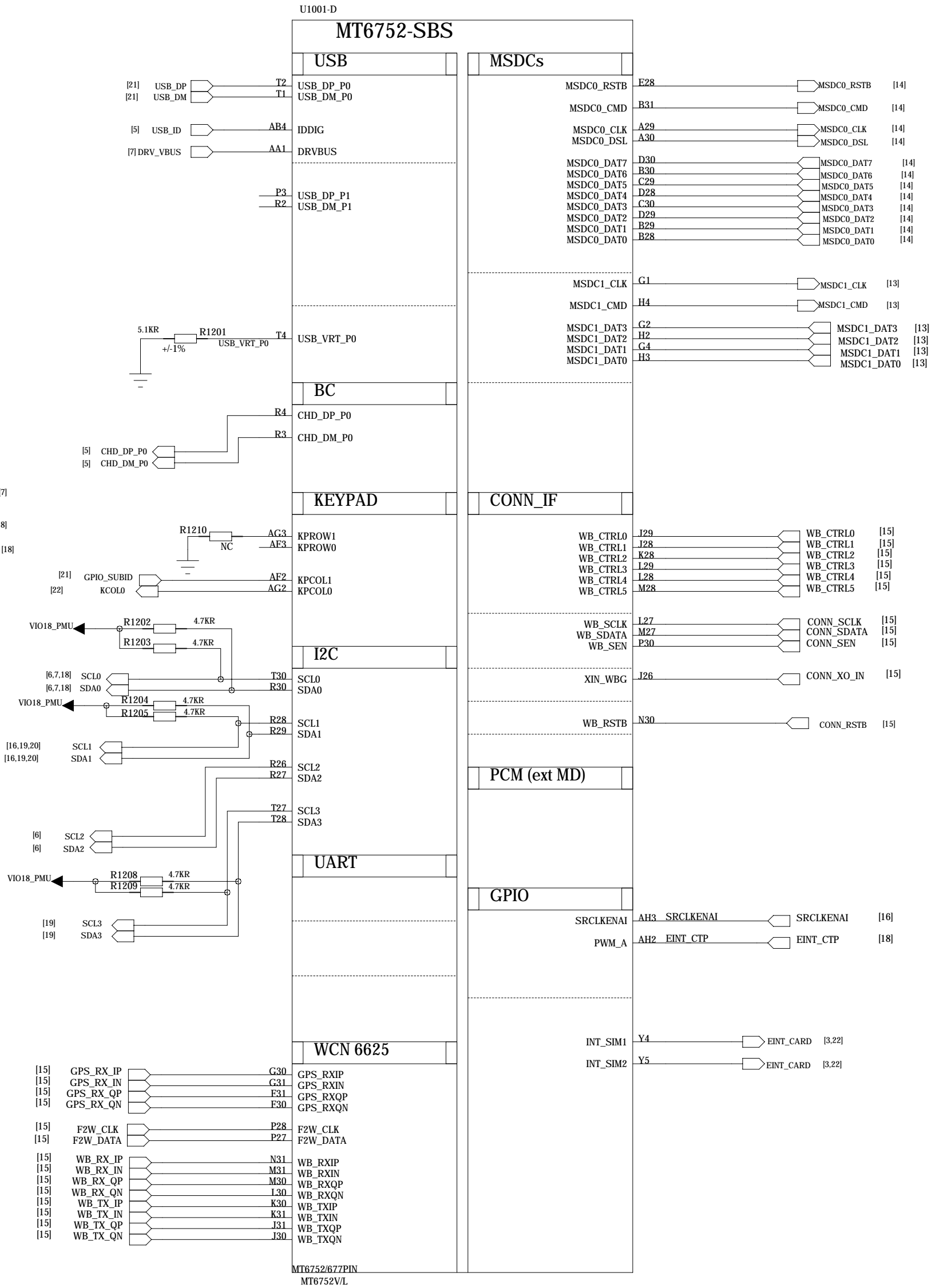
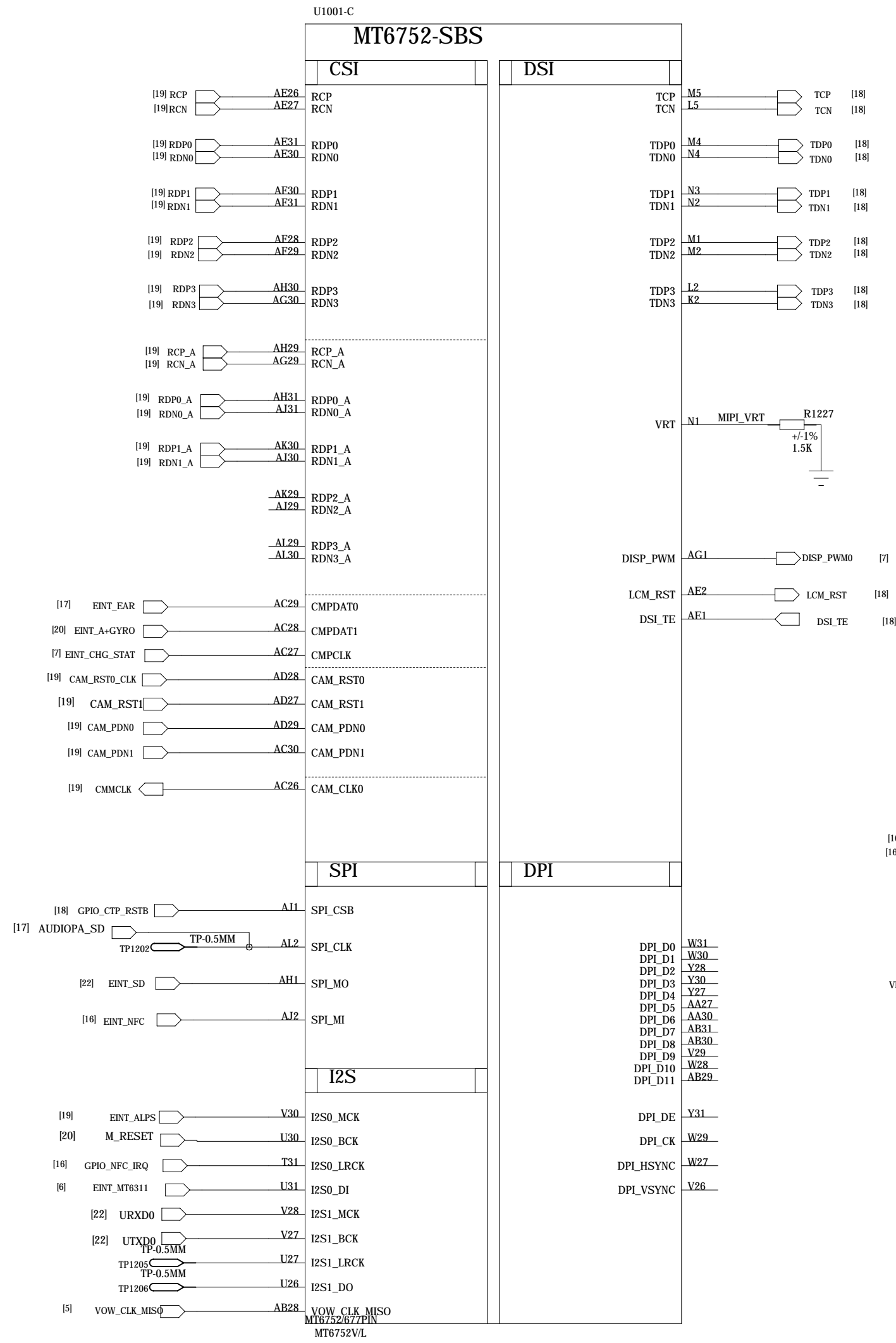
PWRAP_SPI0_CSN	AUD_DAT_MOSI	JTAG
HI	LO	N/A GPIO default
HI	HI	SPI_CSB/SPI_CLK/SPI_MO/SPI_MI
LO	LO	CAM_CLK0/CAM_RST0/CAM_RST1/CAM_PDN0
LO	HI	MSDC1_CLK/MSDC1_CMD/MSDC1_DAT0/MSDC1_DAT1

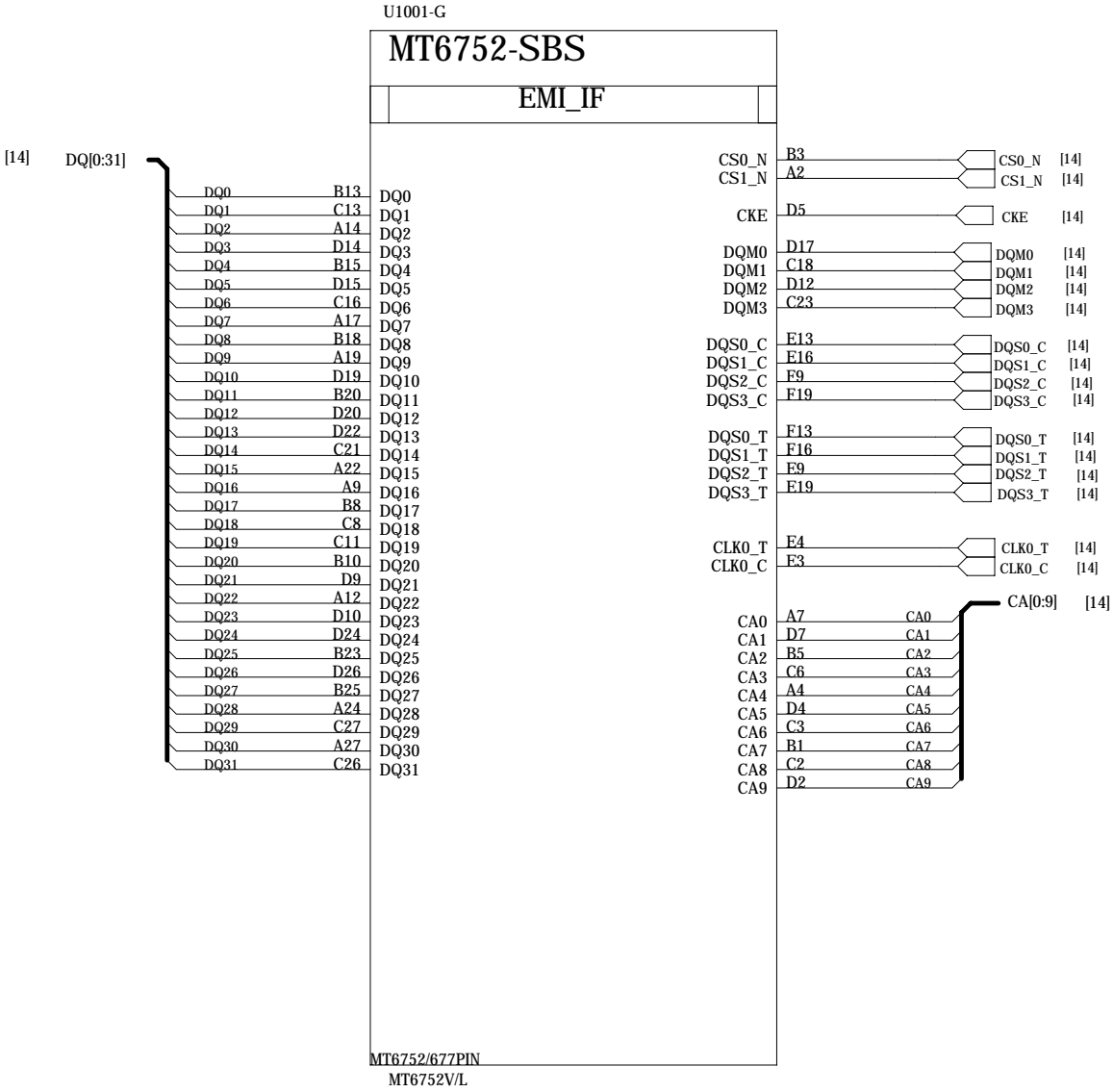
Schematic design notice of "11_BB_1" page.

Note 11-1: The BPI_BUS0~BPI_BUS9 are capable of 2.8V I/O ,according to the input of DVDD28_BPI1 and DVDD28_BPI2

Note 11-2: PWRAP_SPI0_CSN and AUD_DAT_MOSI are JTAG feature in bootstrap.

Note 11-3: The de-coupling cap. of DRAM VREF have to be placed as close to BB as possible.



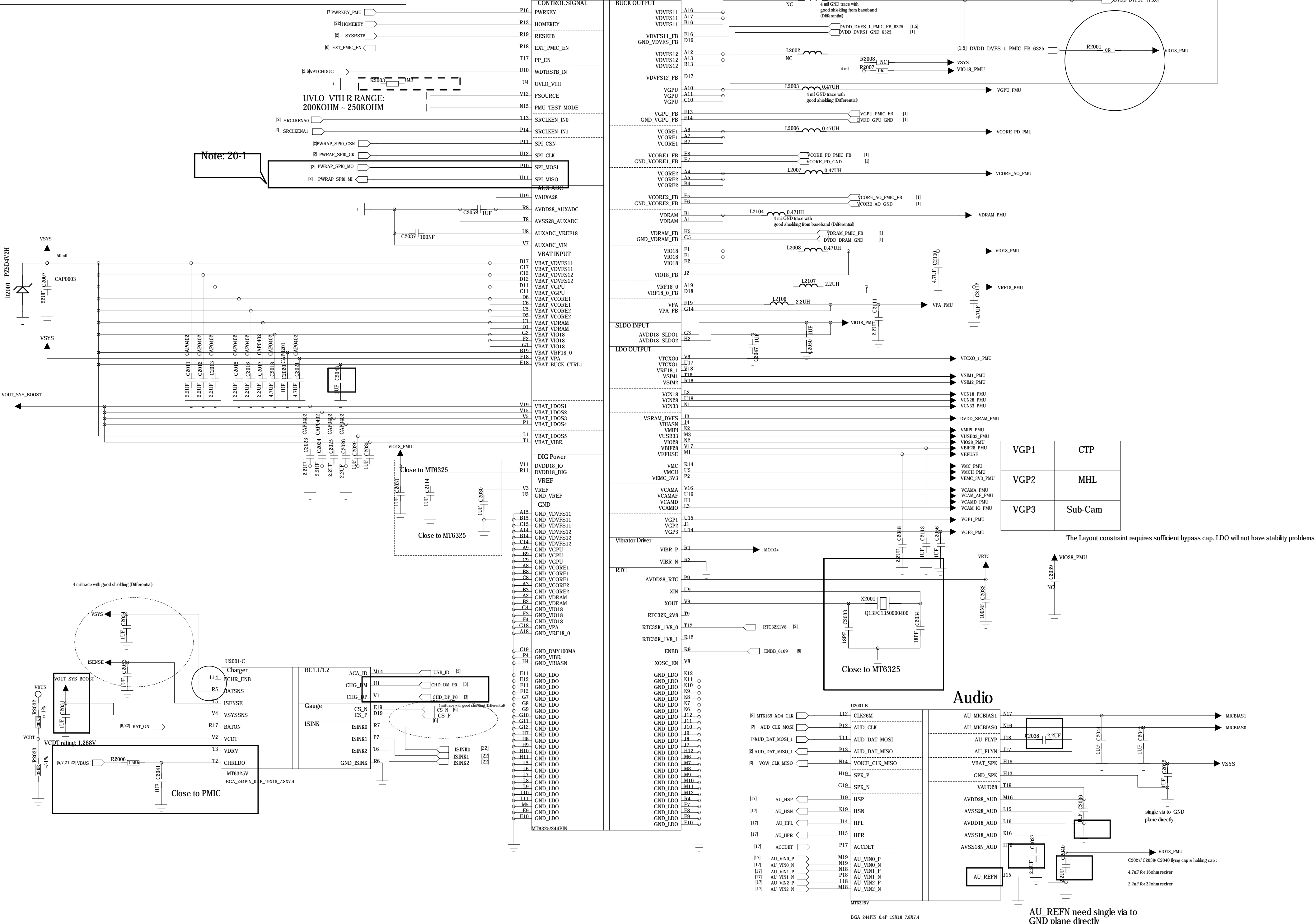


MT6752/677PIN

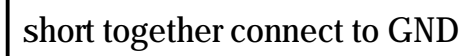
MT6752V/L

Schematic design notice of "20_POWER_MT6325" page.

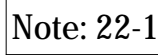
Note 20-1: PAD_PWRAP_SPI0_MI and PAD_PWRAP_SPI0_MO are DRAM feature in bootstrap.



TPS61280 I2C address: 0X75 (Write:0xEA, Read:0xEB)

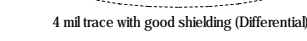


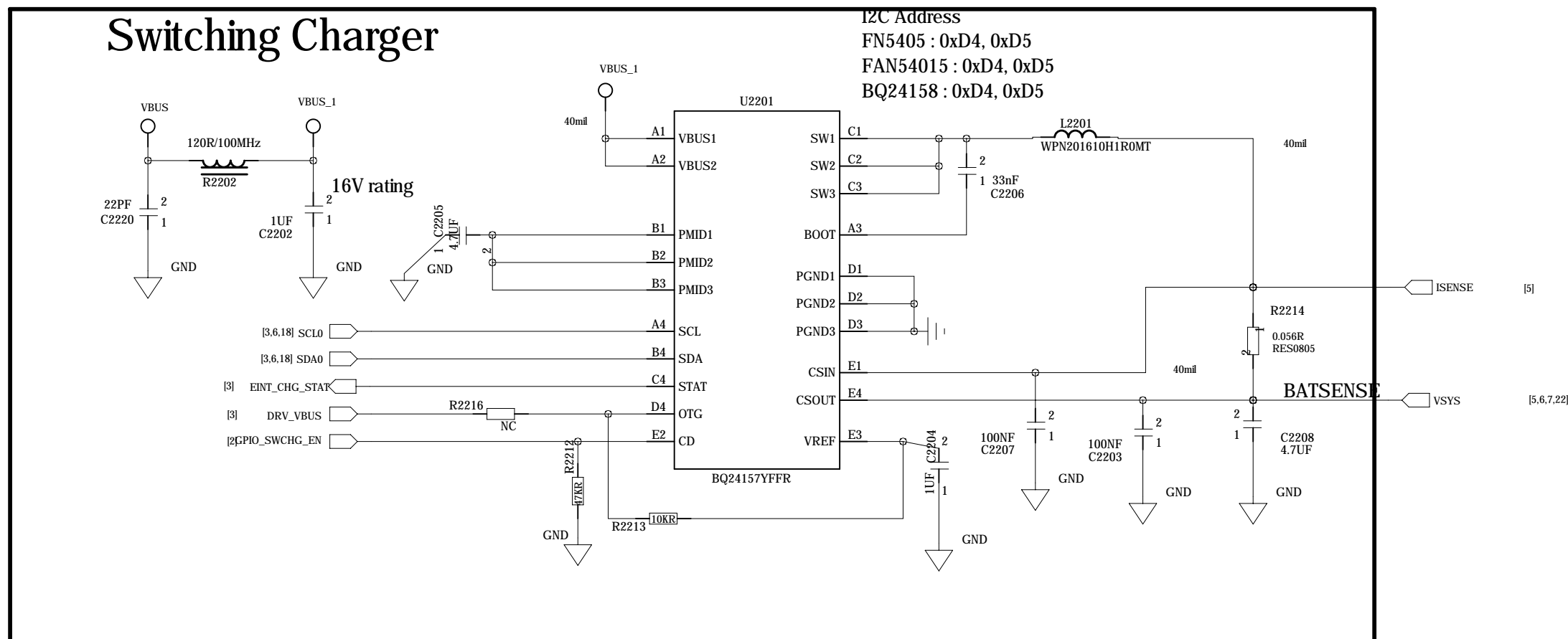
MT6311 / 2-Phase Buck I2C address: 0X6B (Write:0x, Read:0x)



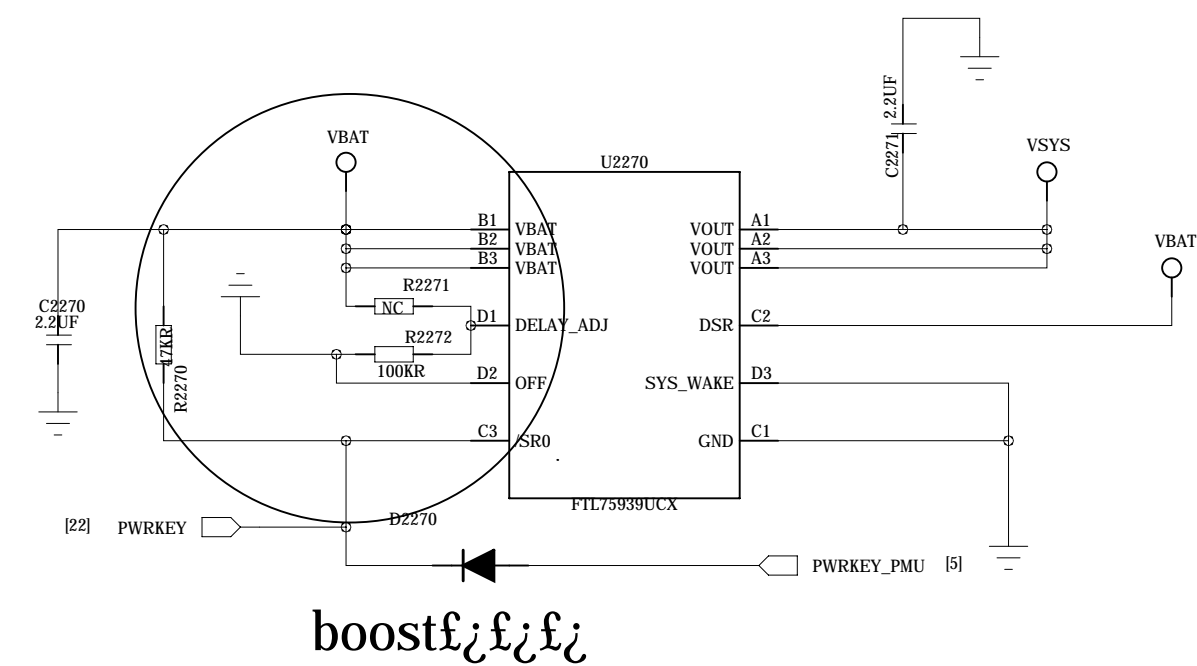
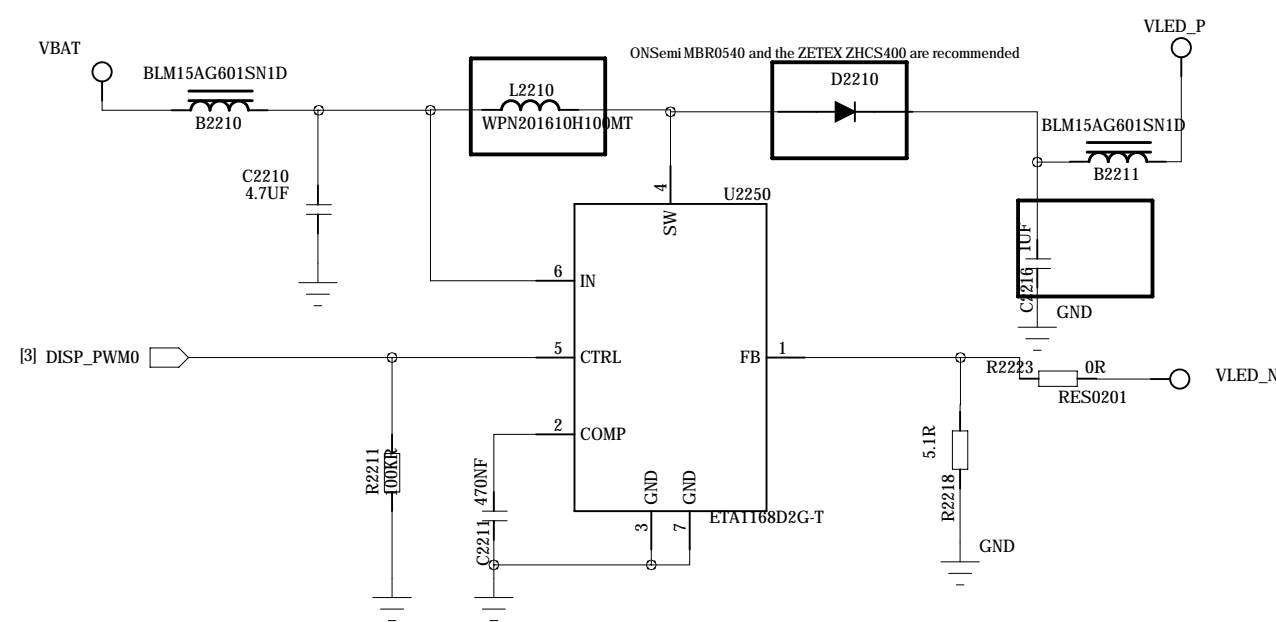
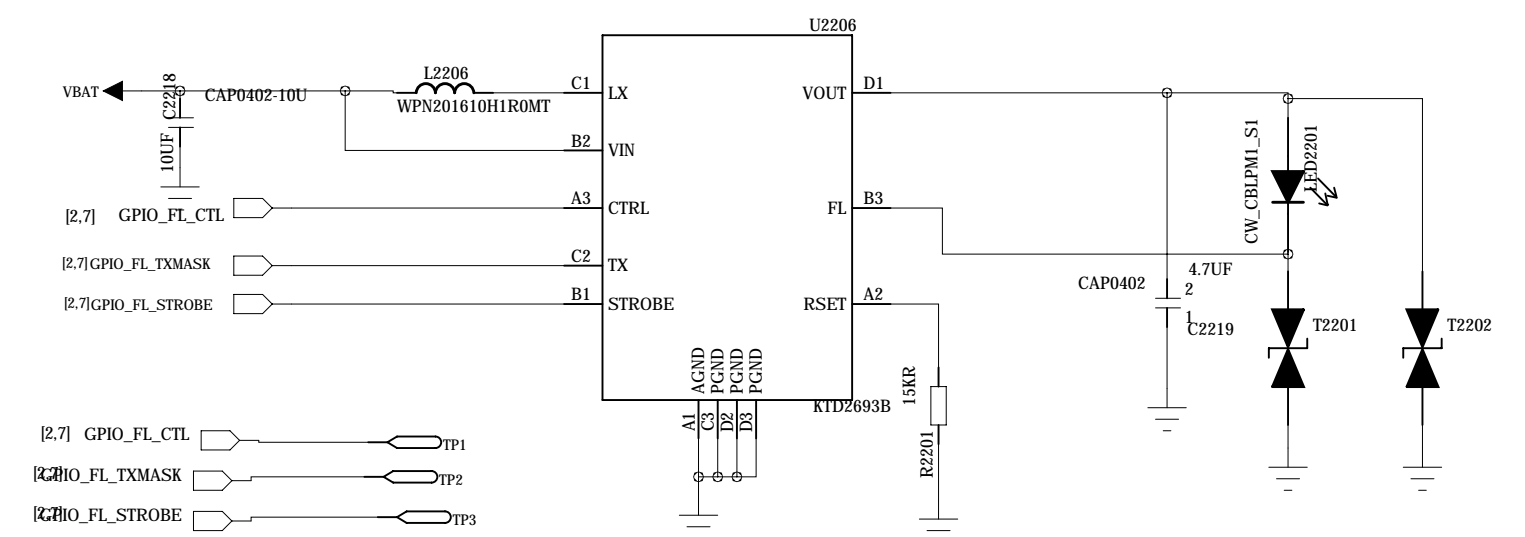
8 Core DVFS FB setting (8 Core and 4 Core Co-Layout)

Note 22-1: MT6311 => Buck EN controlled by EXT_PMIC_EN from MT6325 and I2C.





Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)



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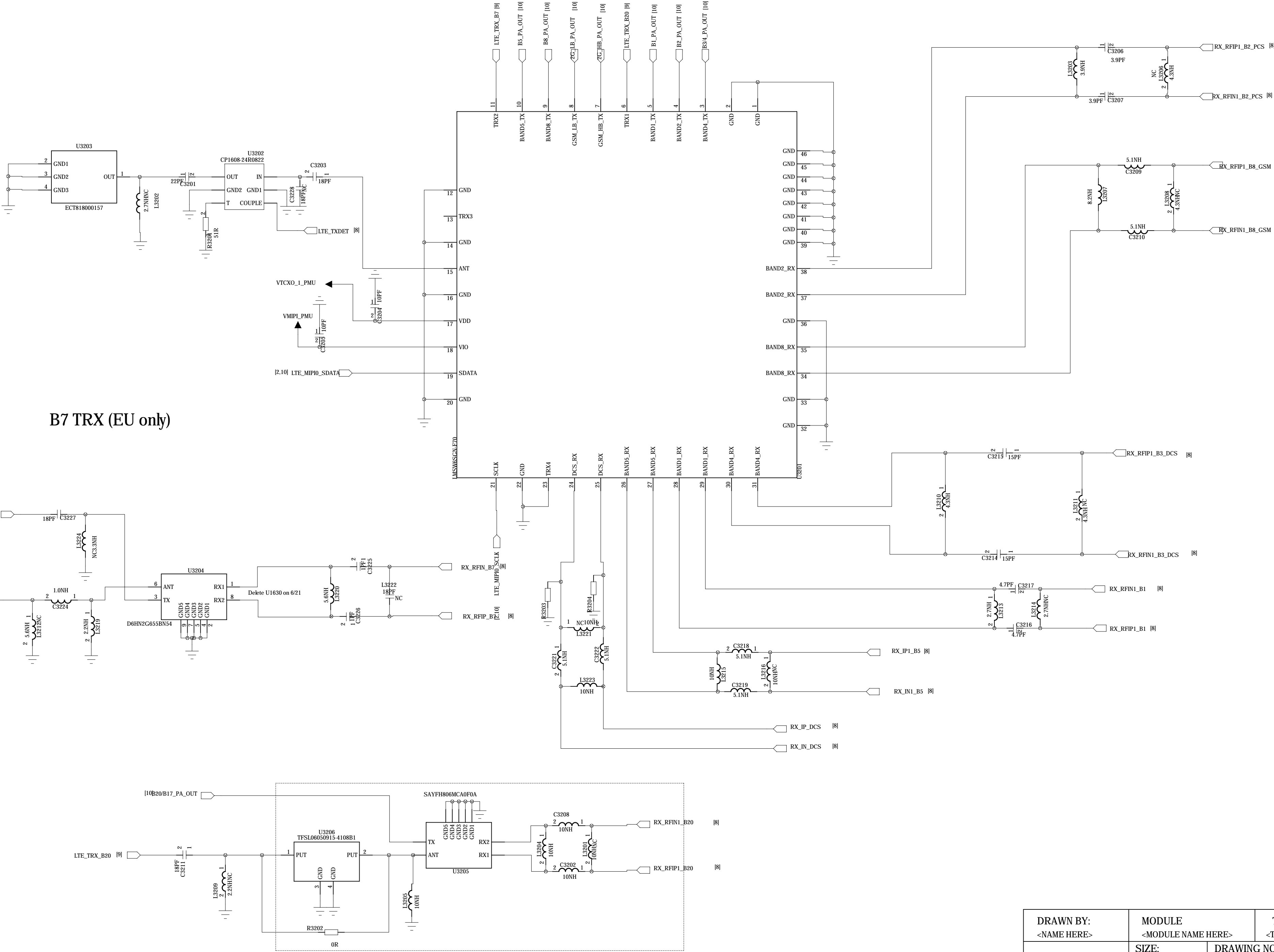
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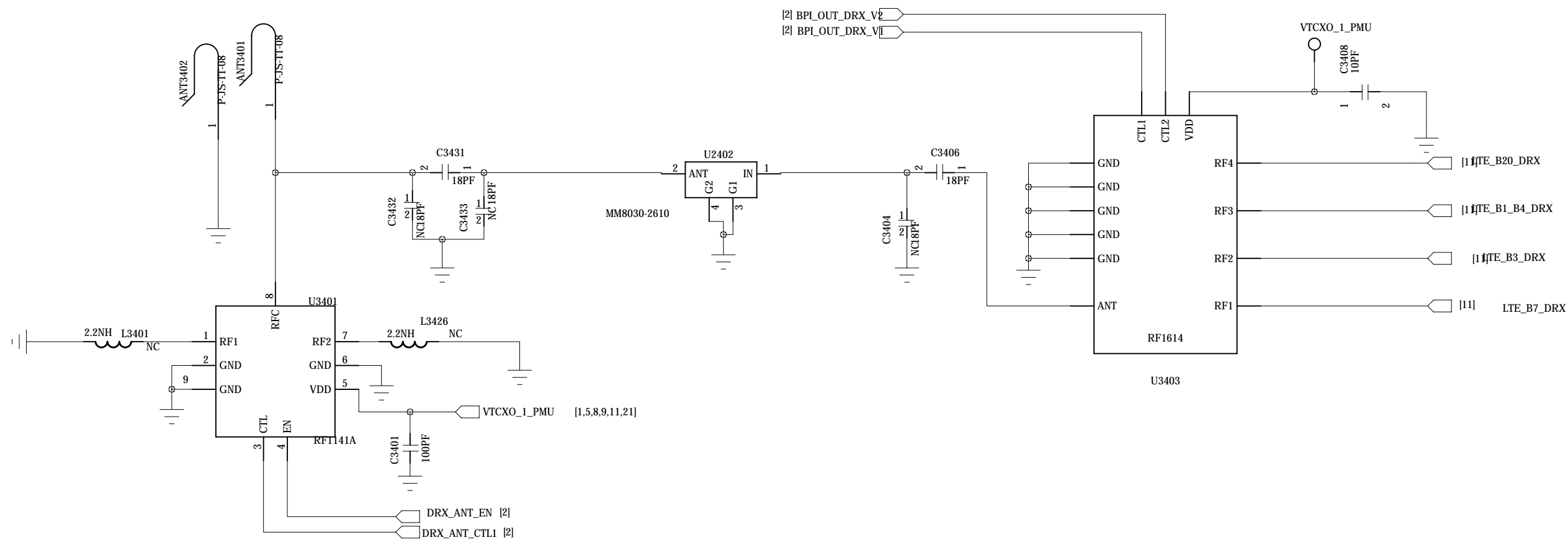
C

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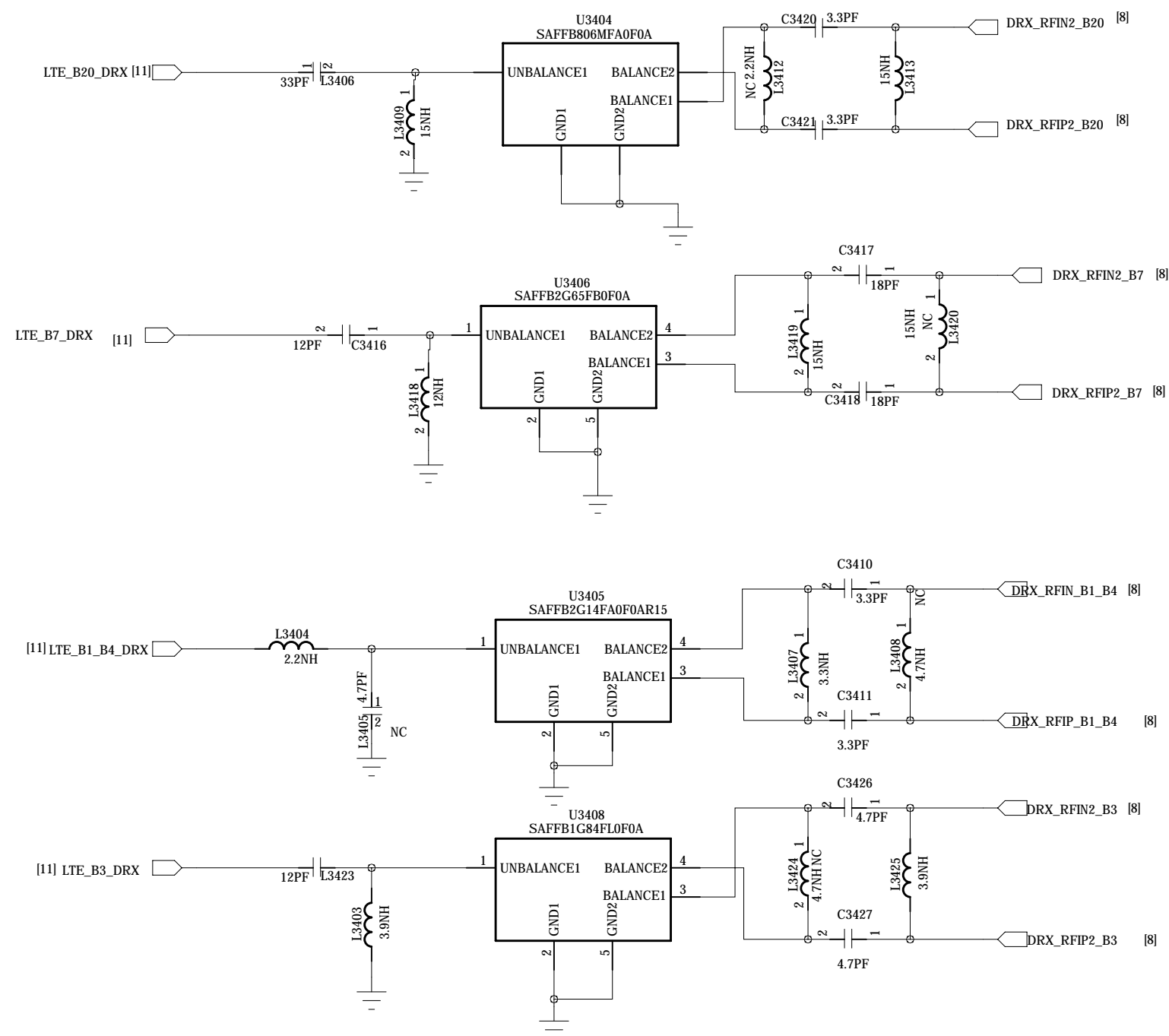
A



DRAWN BY: <NAME HERE>	MODULE <MODULE NAME HERE>	TITLE: <TITLE NAME HERE>	
CHECKED BY: <NAME HERE>	SIZE: A2	DRAWING NO: <DRAWN NO HERE>	REV: <NO>
SHEET: No of No		<DATE HERE>	



B20 DRX(EU)

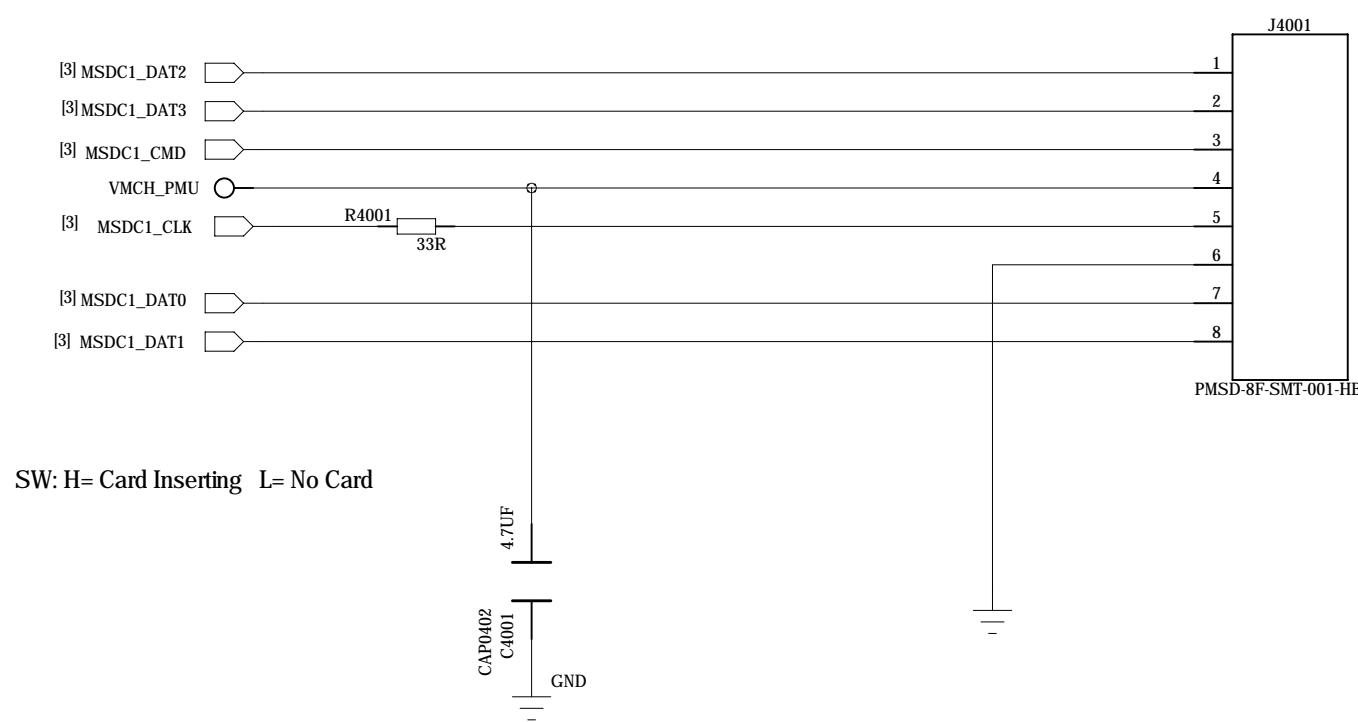


B1/4 DRX (EU & LATAM)

B3 DRX(EU)
B2 DRX(LATAM)

DRAWN BY: <NAME HERE>	MODULE <MODULE NAME HERE>		TITLE: <TITLE NAME HERE>
CHECKED BY: <NAME HERE>	SIZE: A2	DRAWING NO: <DRAWN NO HERE>	REV: <NO>
	SHEET: No of No <DATE HERE>		

TFlash card

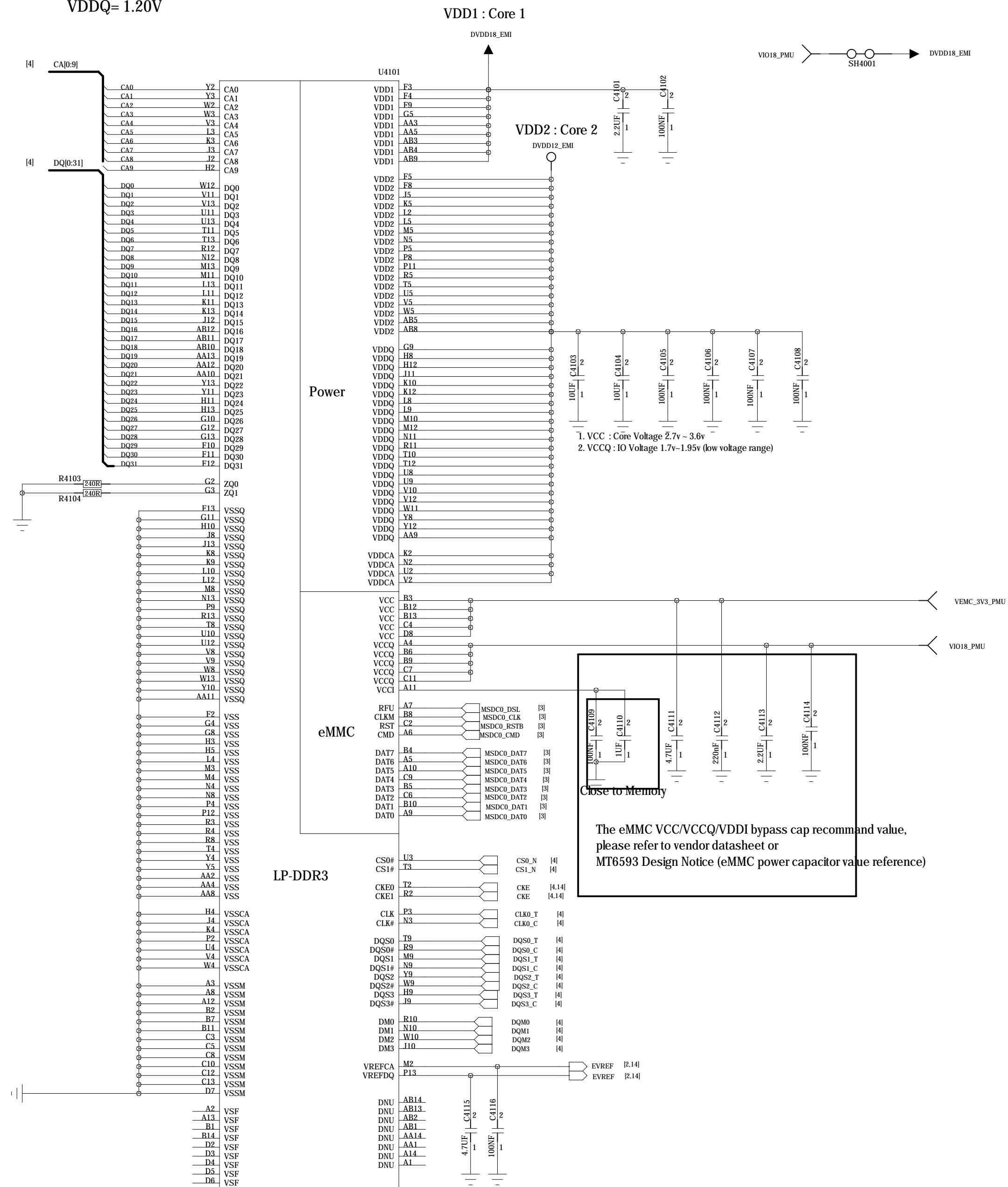


Schematic design notice of "41_MEMORY_SD Card" page.

Note 41-1: The equivalent capacitance of ESD protection device must be <=0.5pF
 -- otherwise it will result in NFC card mode function fail.

16GB eMMC + 16Gb LPDDR3

VDD1=1.8V
VDD2=1.20V
VDDCA=1.2V
VDDQ= 1.20V



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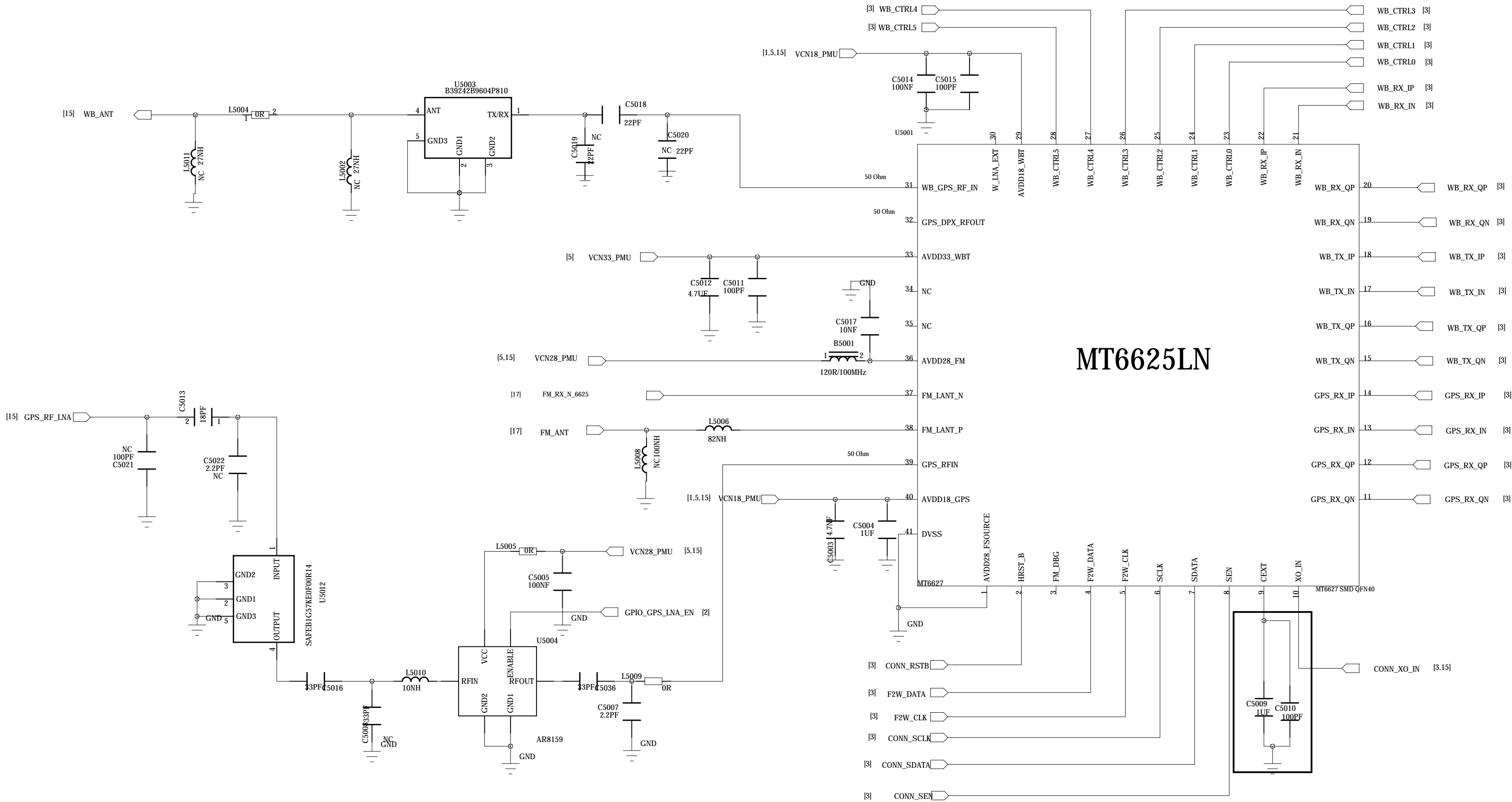
A

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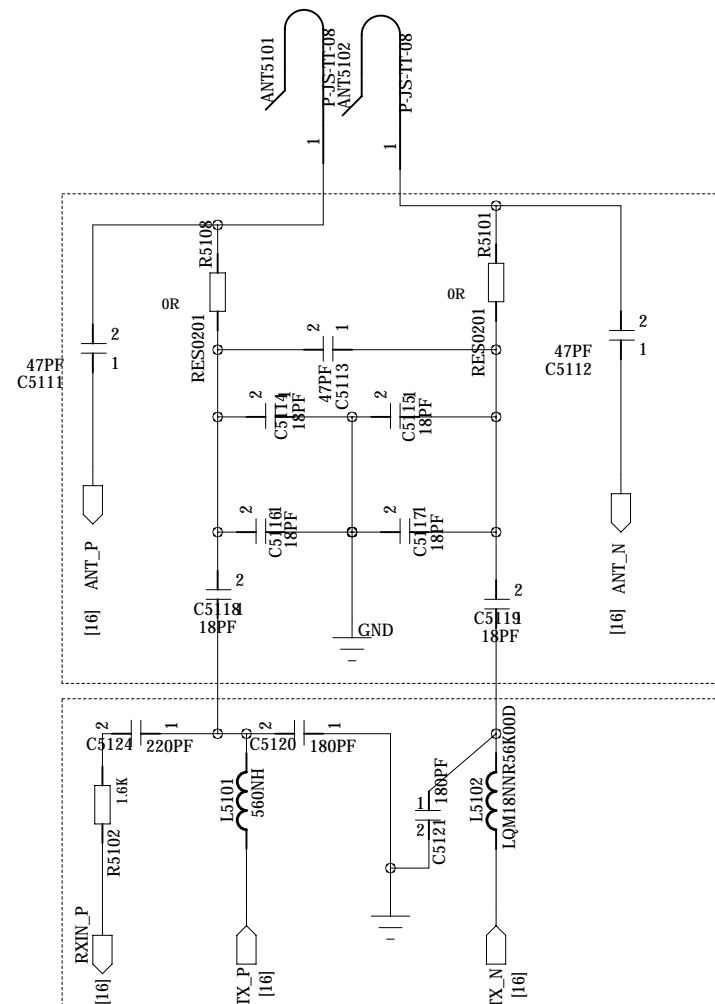
A



MT6625LN

DRAWN BY: <NAME HERE>	MODULE <MODULE NAME HERE>		TITLE: <TITLE NAME HERE>	
CHECKED BY: <NAME HERE>	SIZE: A2	DRAWING NO: <DRAWN NO HERE>		REV: <NO>
	SHEET: No of No			

NFC MT6605



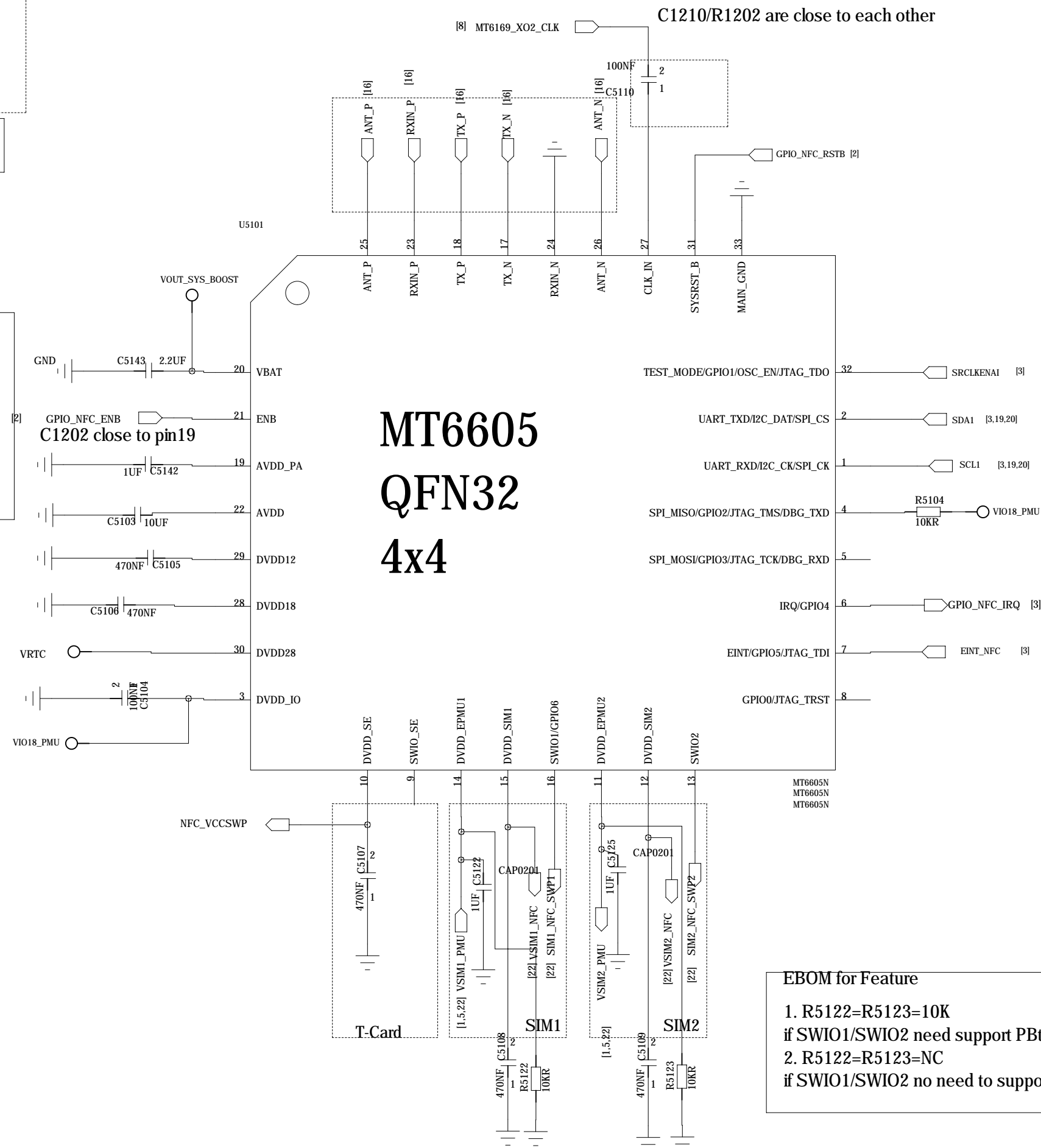
Components in this region
use 5% accuracy

ENB (NFC_VEN)
1.Input pin
2.Internal pull low
3.Low active
4.If default NFC
would like to disable,
please configure to high

C1211,C1212,C1213,C1214,C1215,C1216,C1217, C1218,
C1219 need to use 2% accuracy and 50V tolerance capacitor,
PS: 0201 cap can't tolerance 50V

POWER MODE[1:0]=[NFC_RST:NFC_VENB]

Power Mode	NFC_RST	NFC_VENB
NFC enable (configure, R/W, card, polling loop, polling loop card listening)	1	0
NFC disable (HPD)	0	1
High battery card listening	1	1
Reset	0	0



SYSRST_B (NFC_RST)
1. Input pin
2. Internal pull high
3. Low active

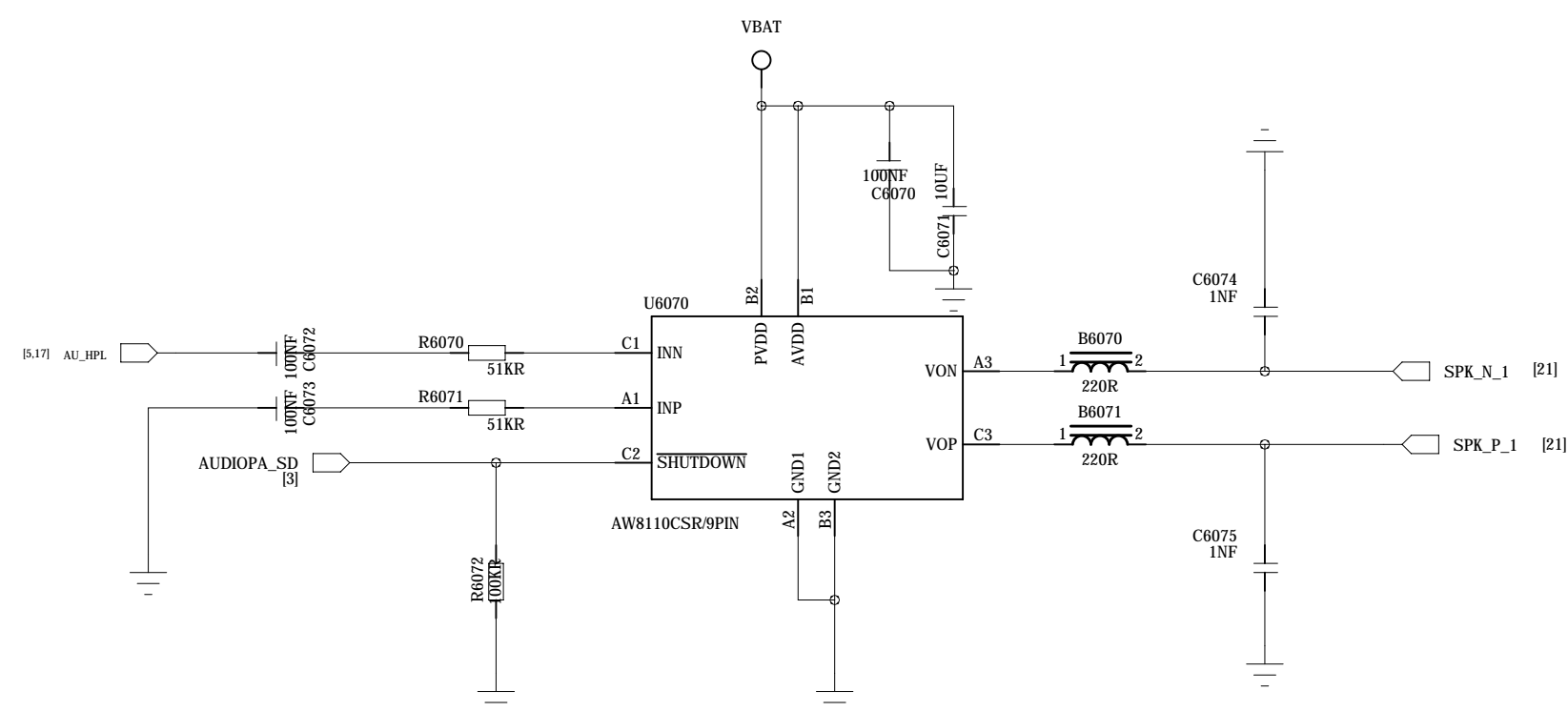
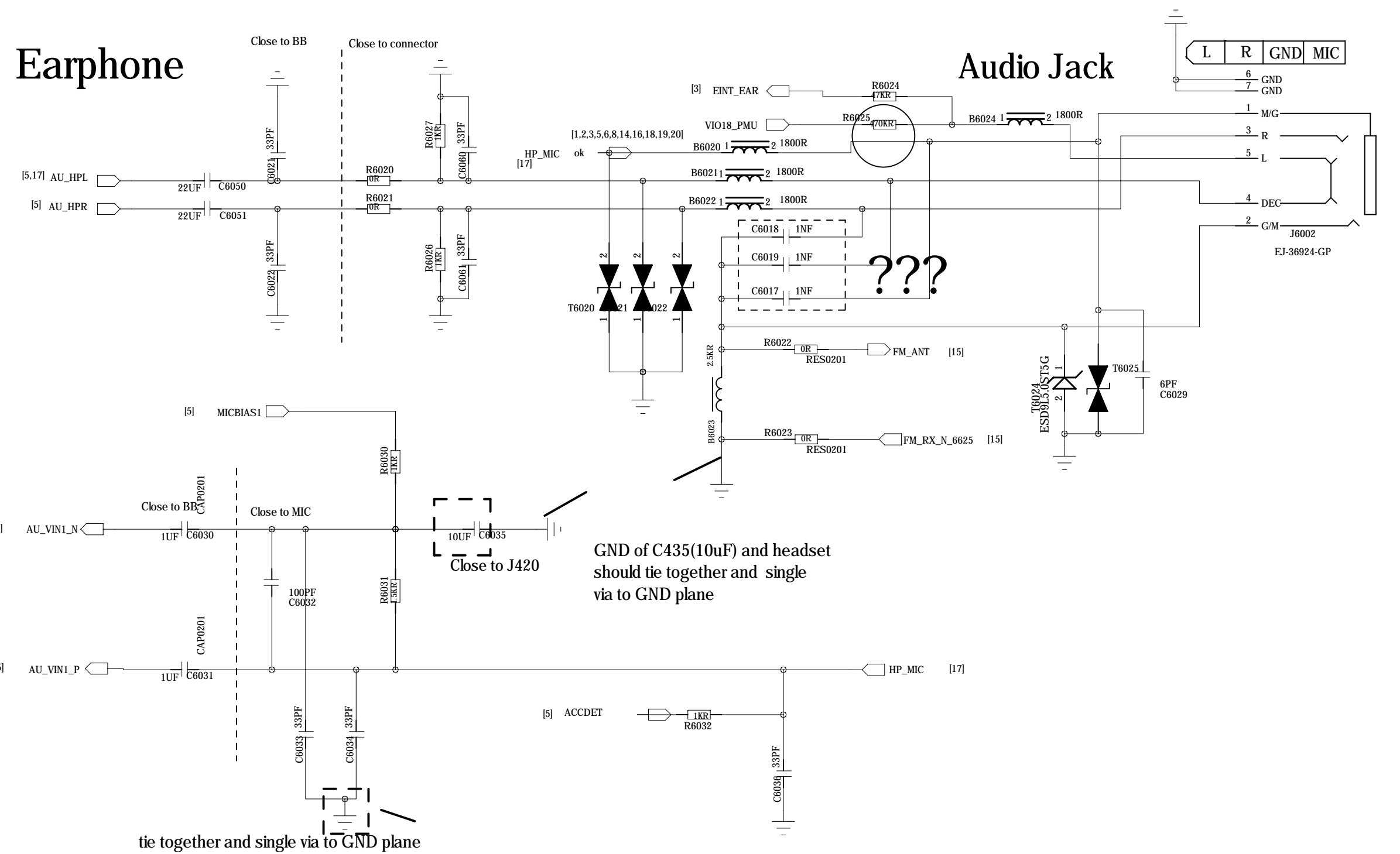
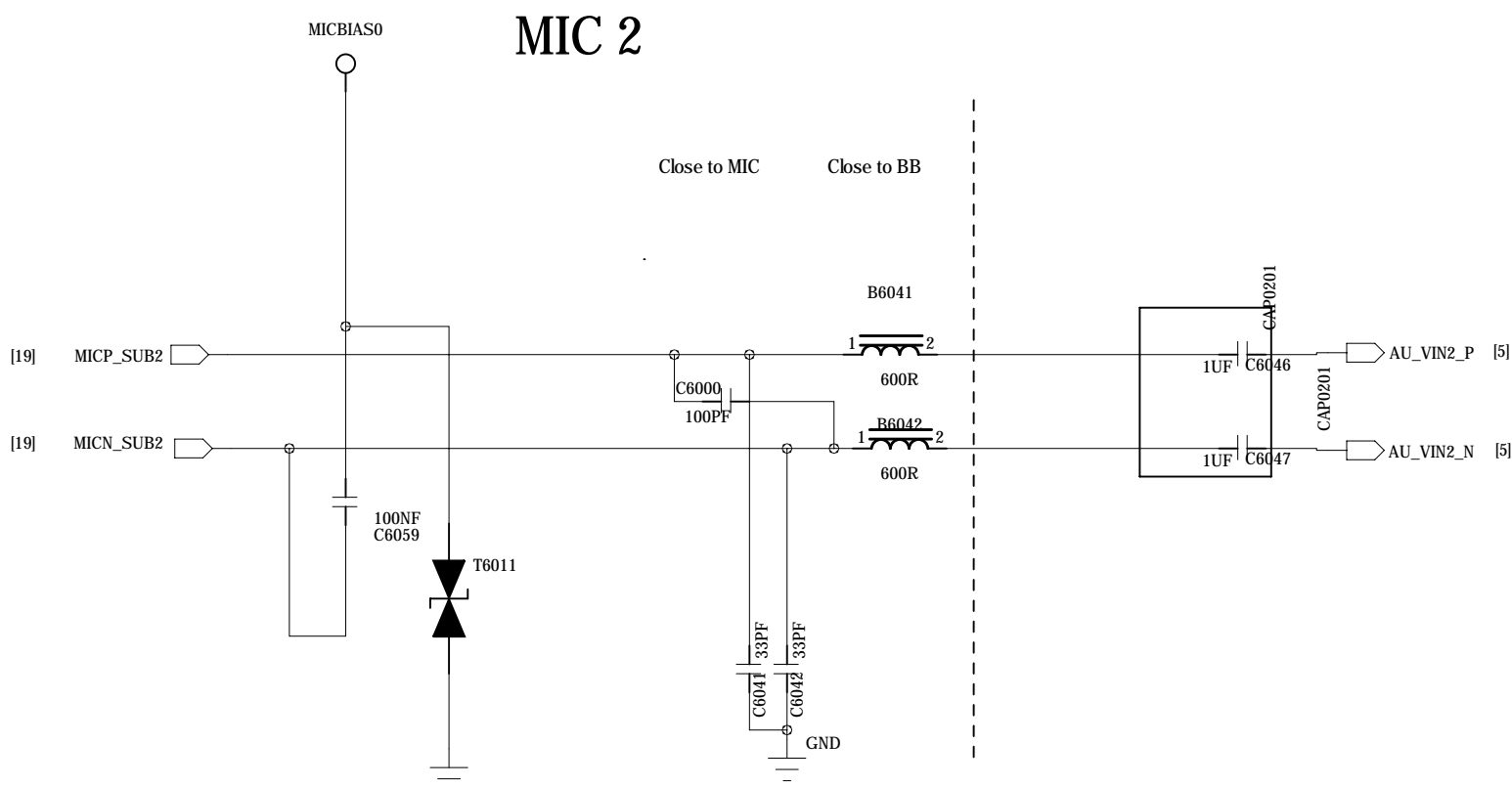
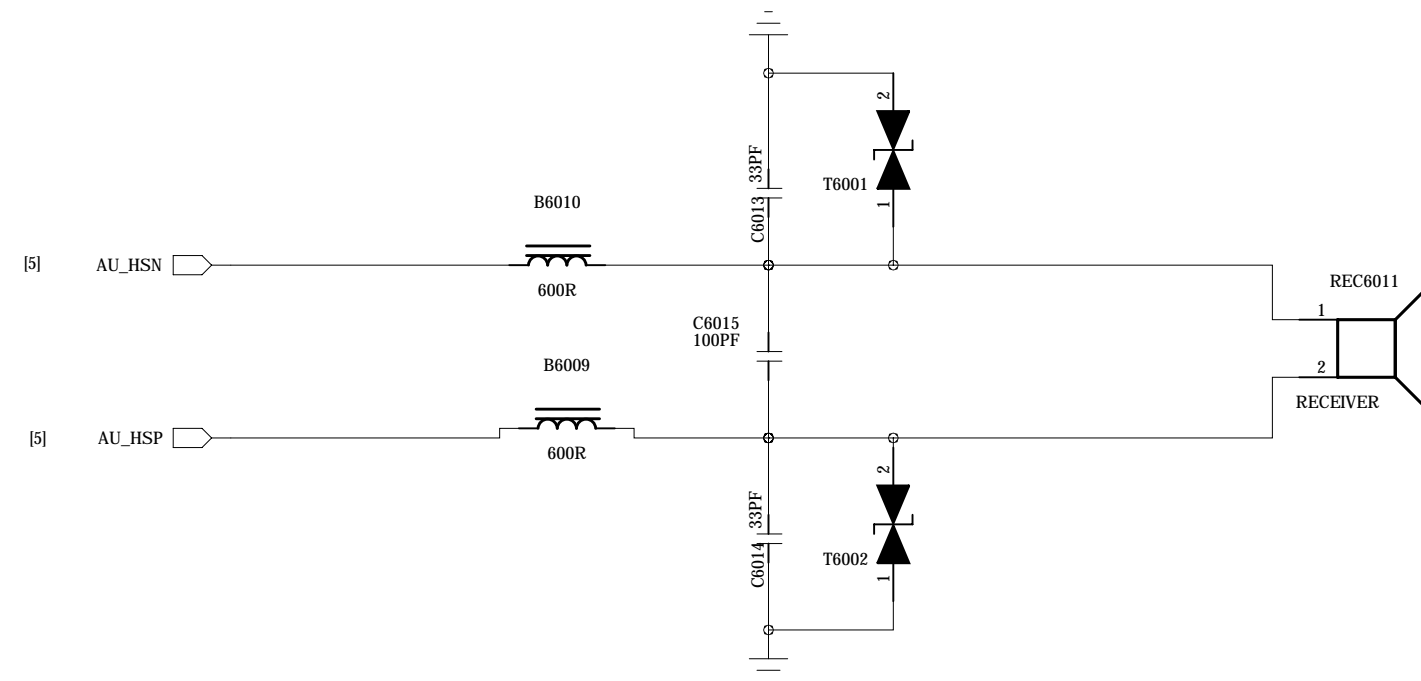
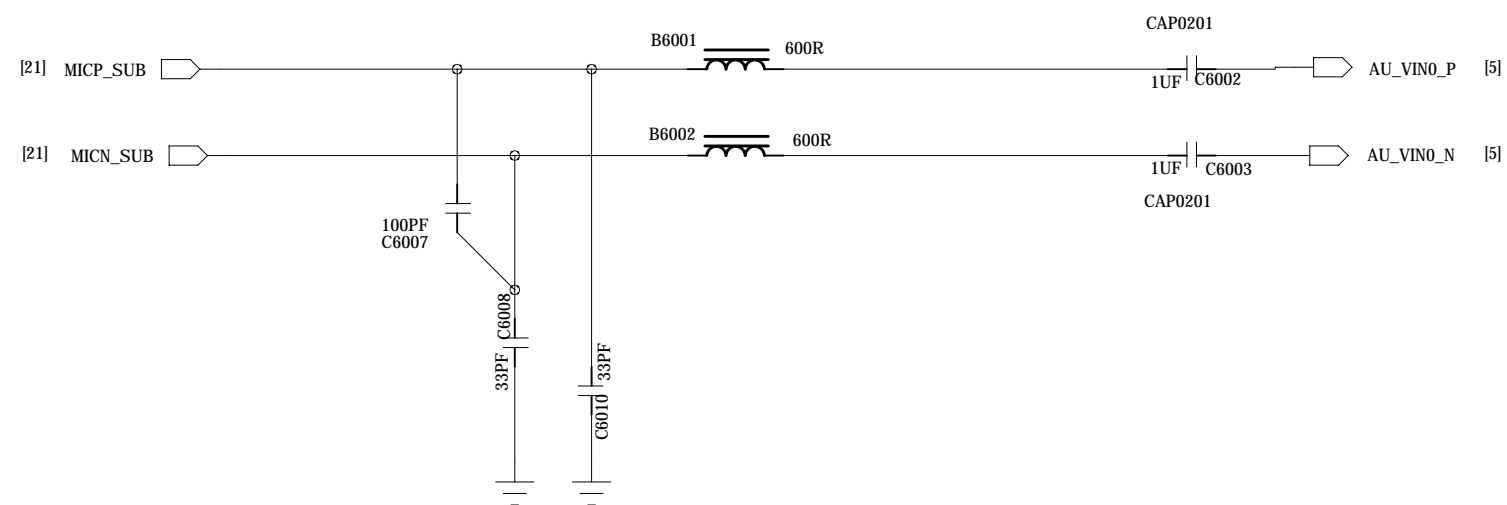
1.NFC_OSC_EN is output pin, and high active. 2.Need to connect to host SRCLKENAI and SRCLKENAI pin need to be default low.
--

Only can use HW I2C. SW I2C is not allowed.	Address:0x28
--	--------------

R1206 NC : XTAL MODE
R1206 10K : Co-Clock

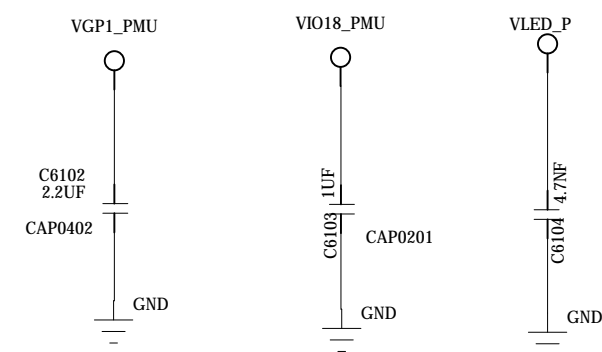
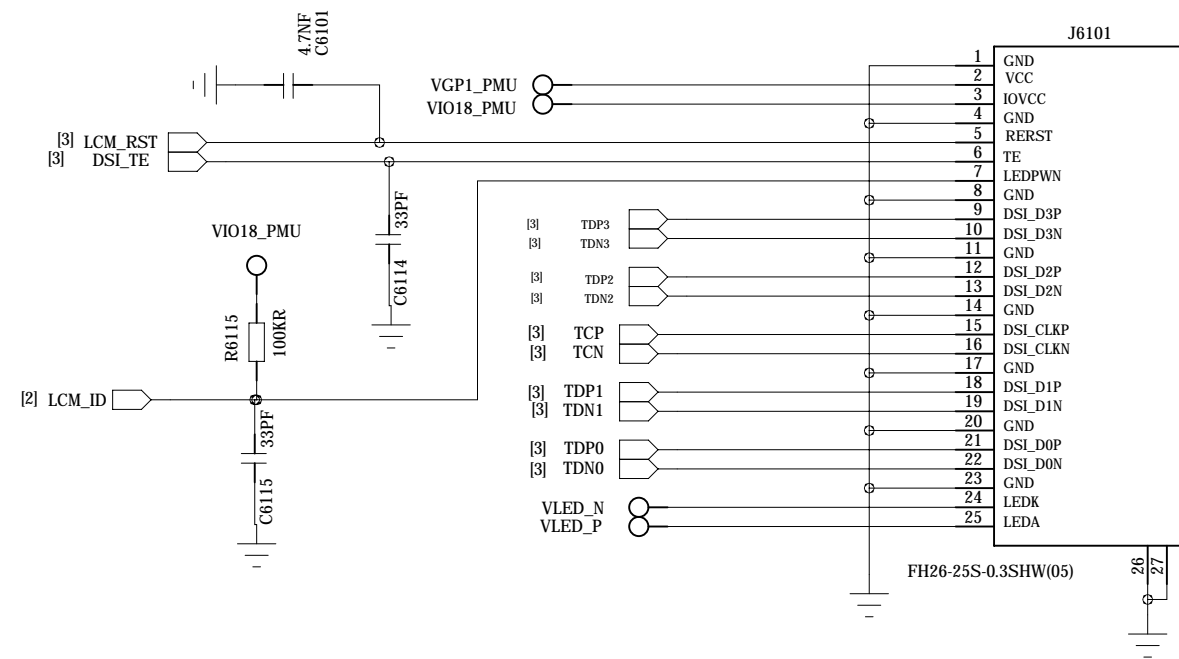
- 1.IRQ_NFC is output pin, and high active.
- 2.IRQ_NFC is also strap pin and host I/F connected with IRQ need to be default low.

EBOM for Feature
1. R5122=R5123=10K if SWIO1/SWIO2 need support PBtF
2. R5122=R5123=NC if SWIO1/SWIO2 no need to support PBtF

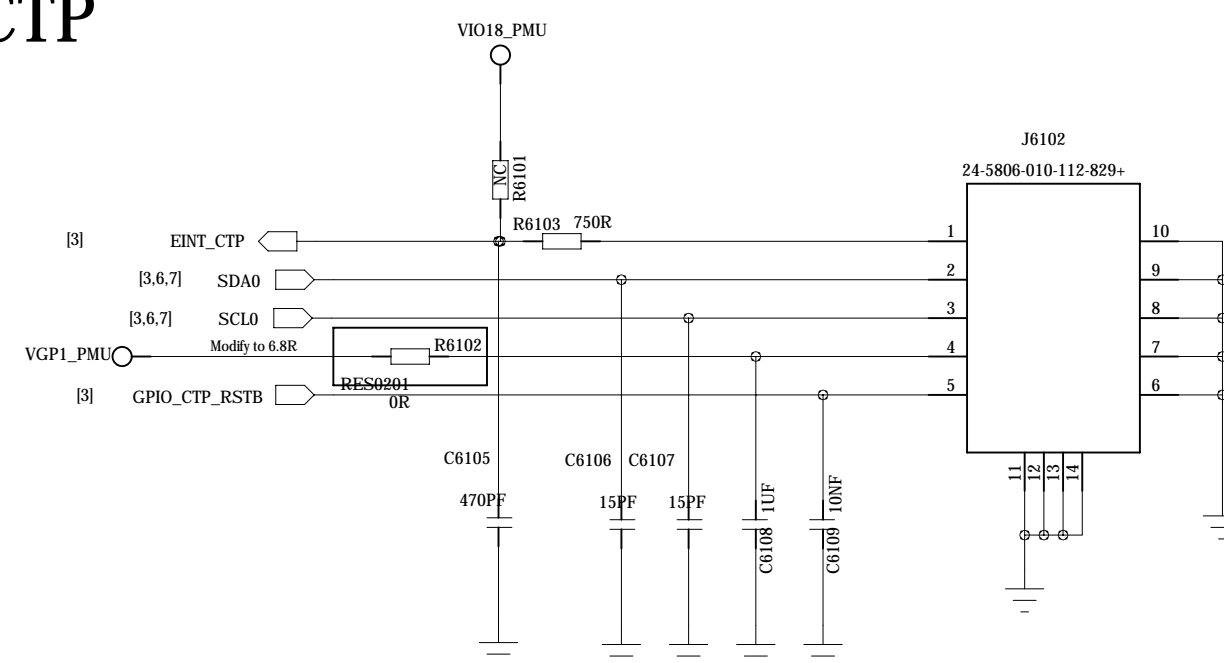


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CHECKED BY: <NAME HERE>	SIZE: A2	ARCHIVING NO: <DRAWN NO HERE>	REV: <NO>	
	SHEET: No of No		<DATE HERE>	

LCM

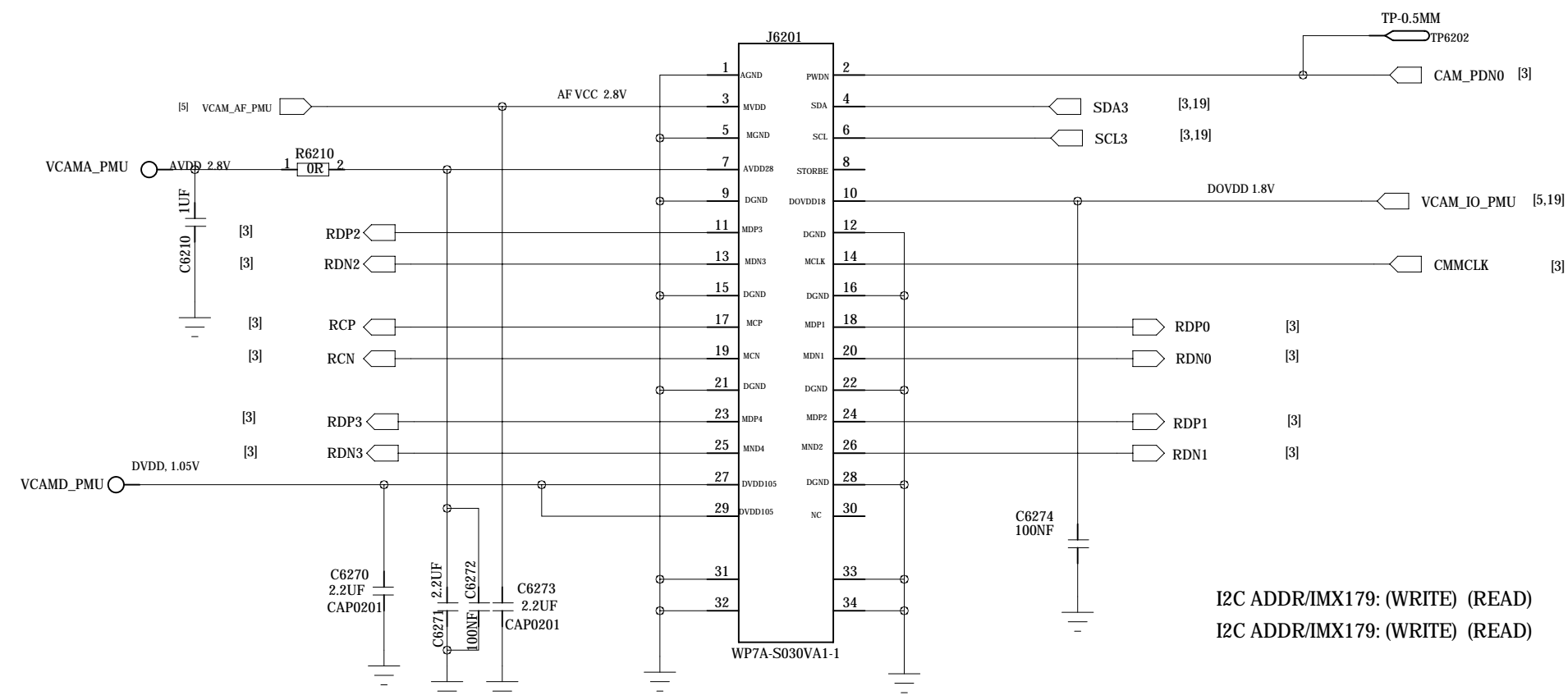


CTP



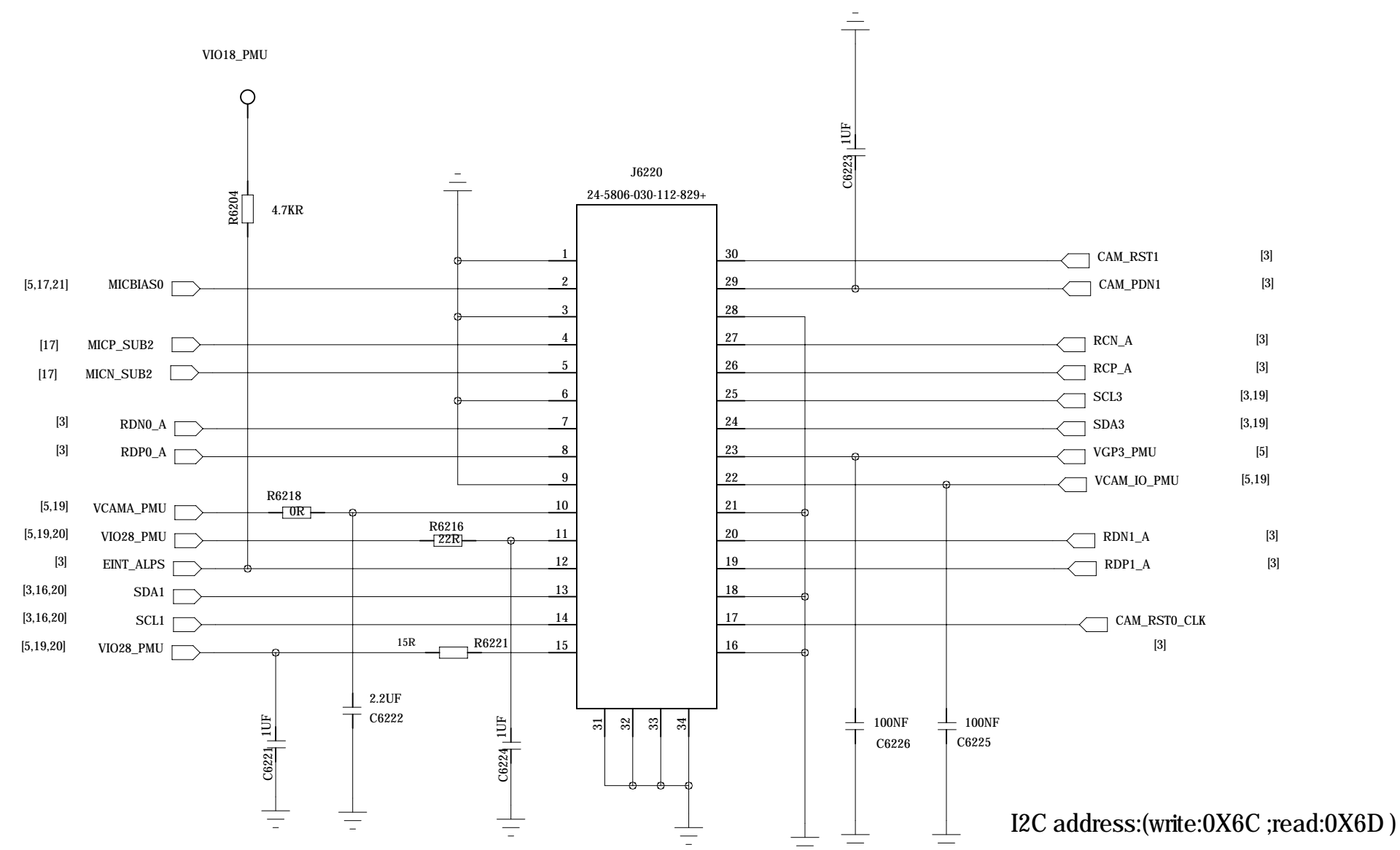
GT917S's INT pin CANNOT be pulled-up.

Main Camera

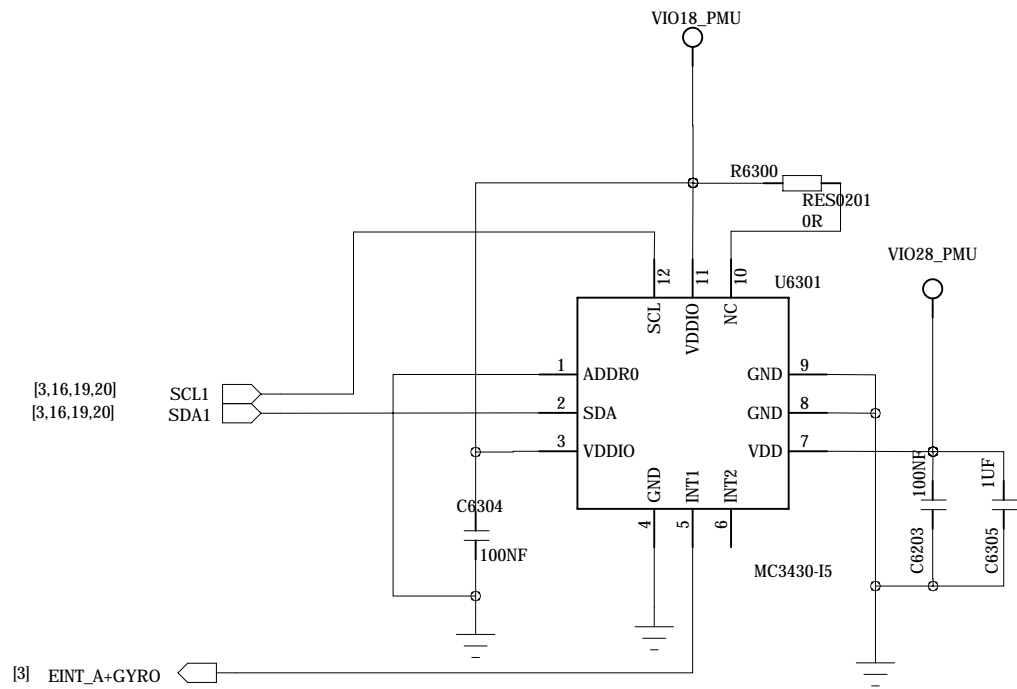


I2C address:(write:0X20 ;read:0X21)

SUB CAM/PS/ALS CON

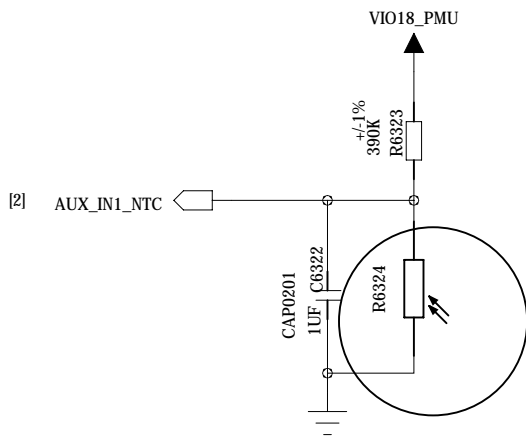
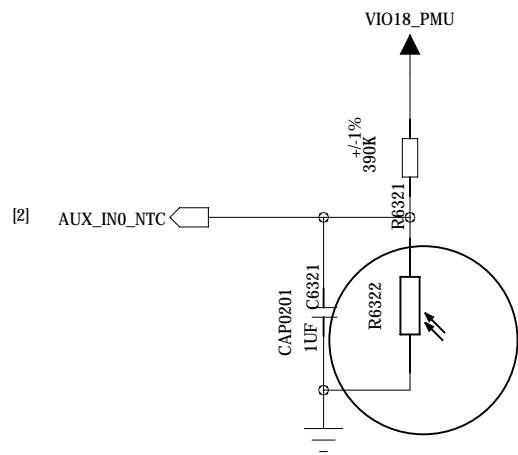
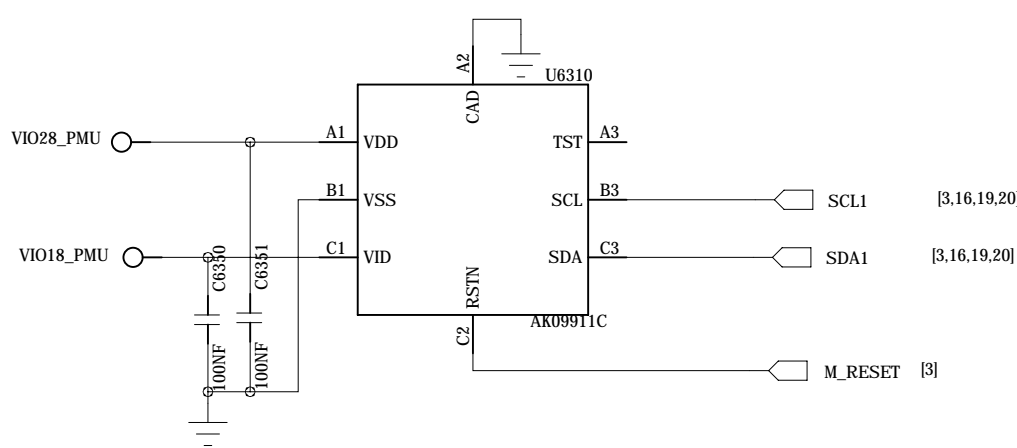


G SENSOR

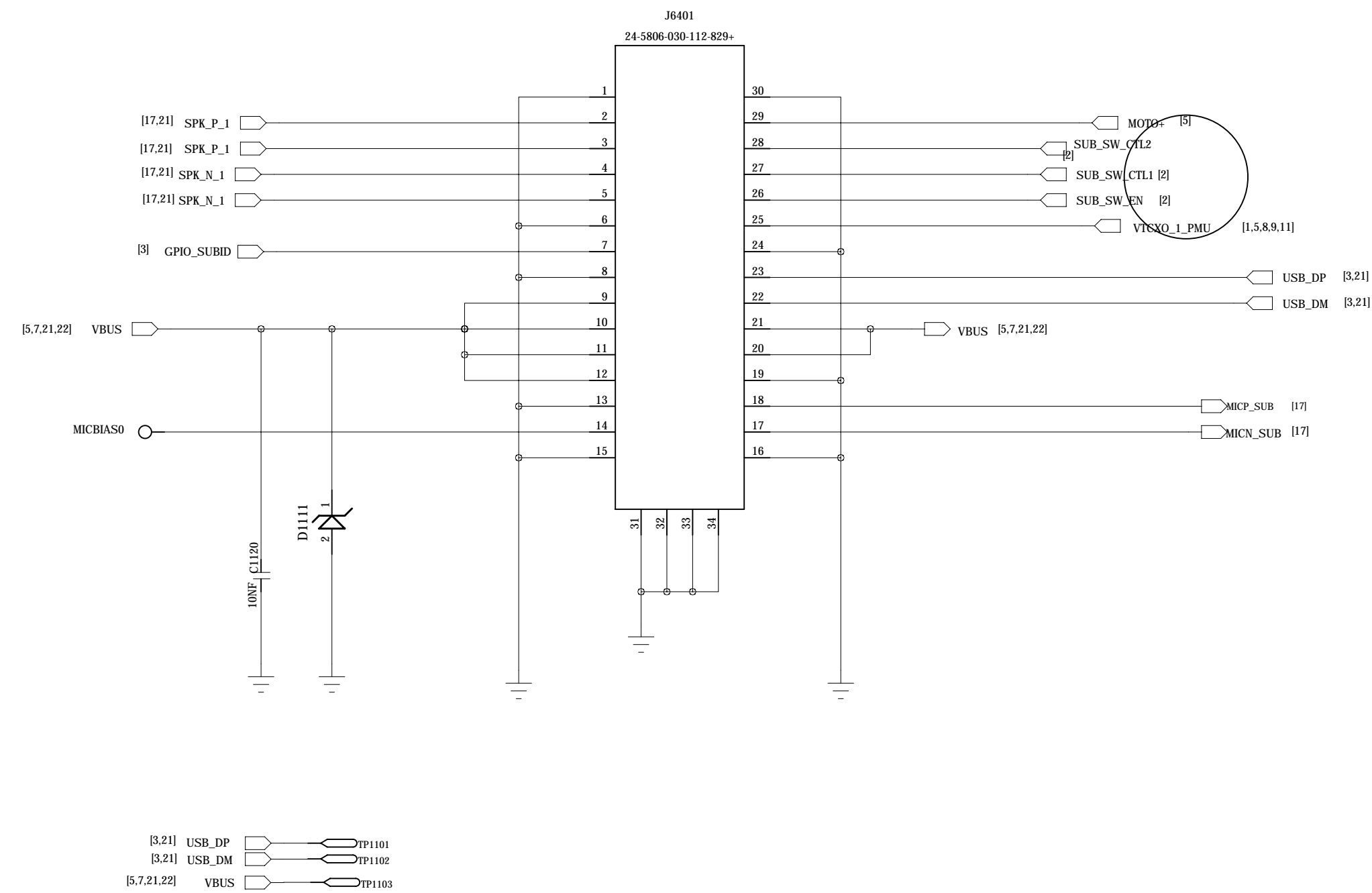


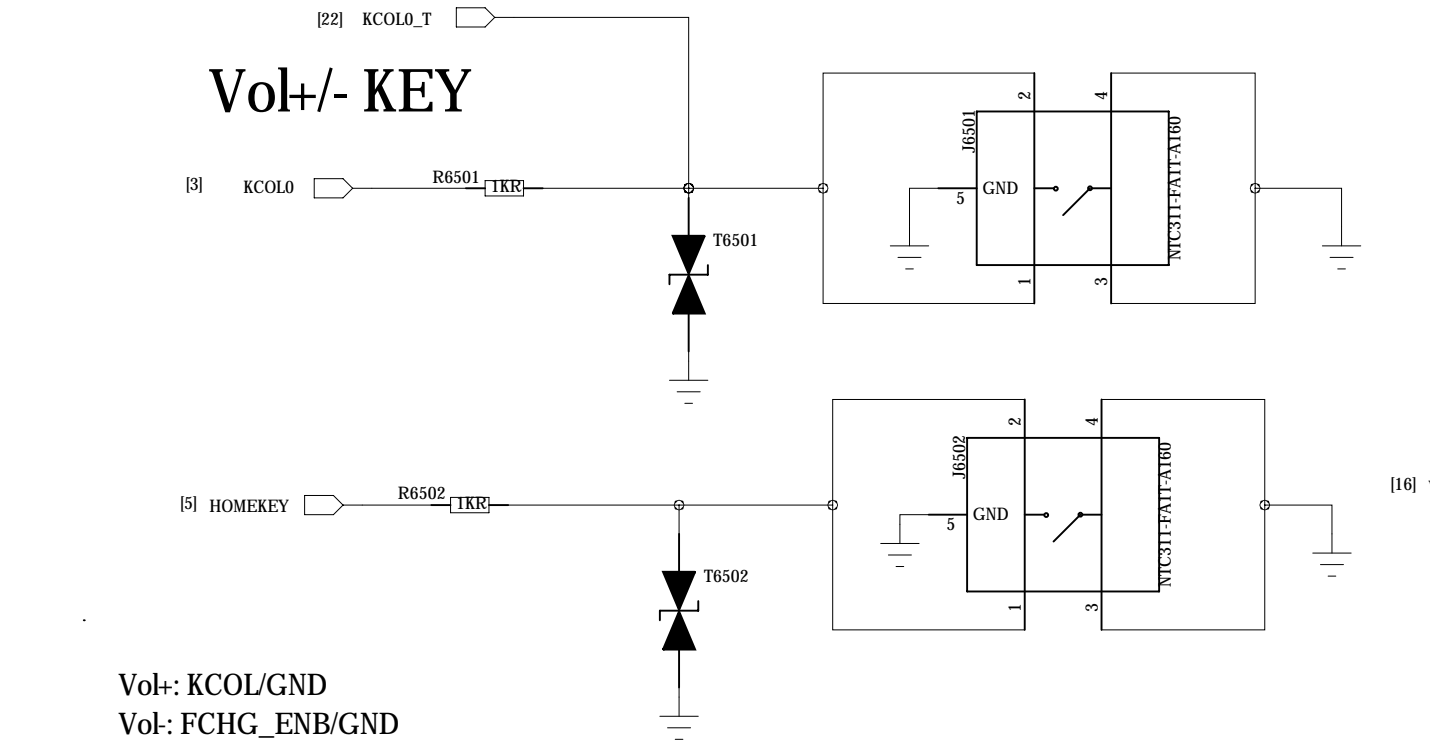
M-SENSOR

I2C address:0x0C(write:0x18;read:0x19)

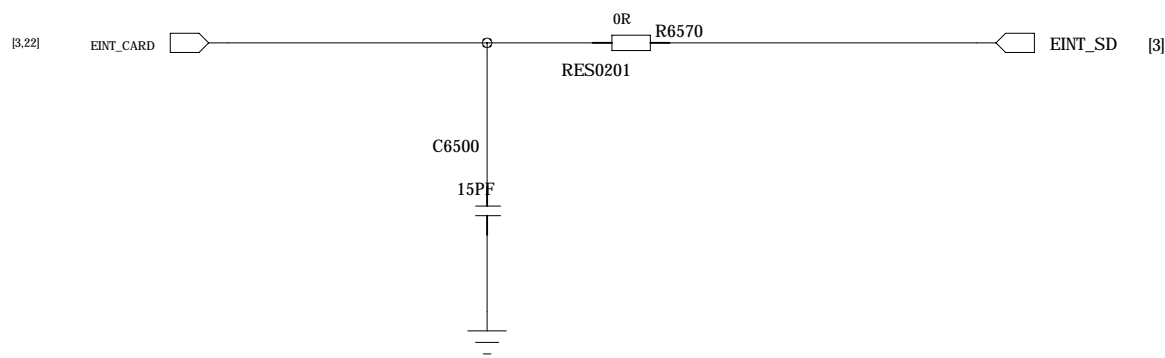
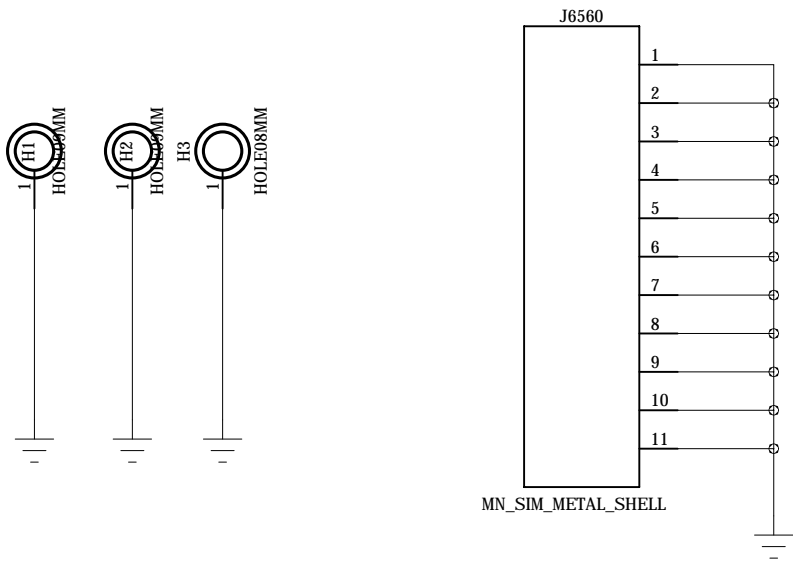
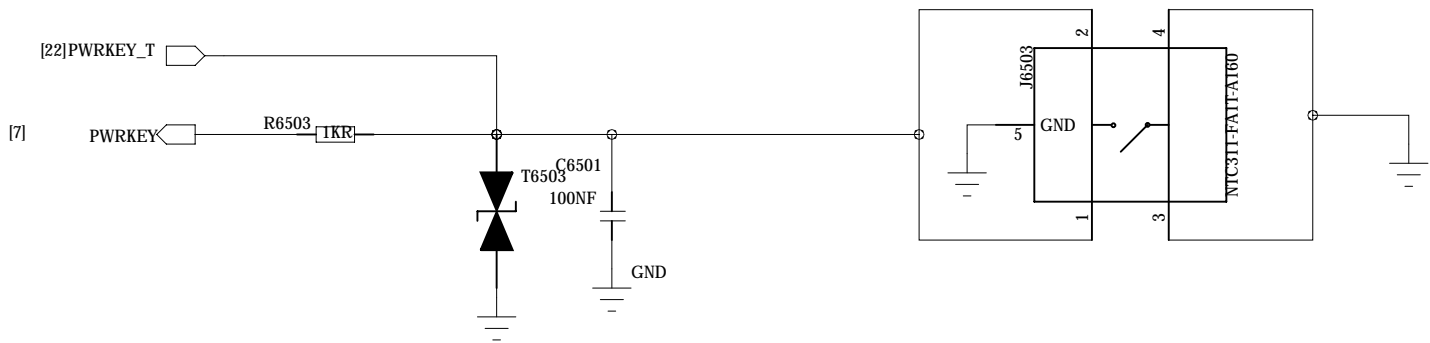


Sub board IO

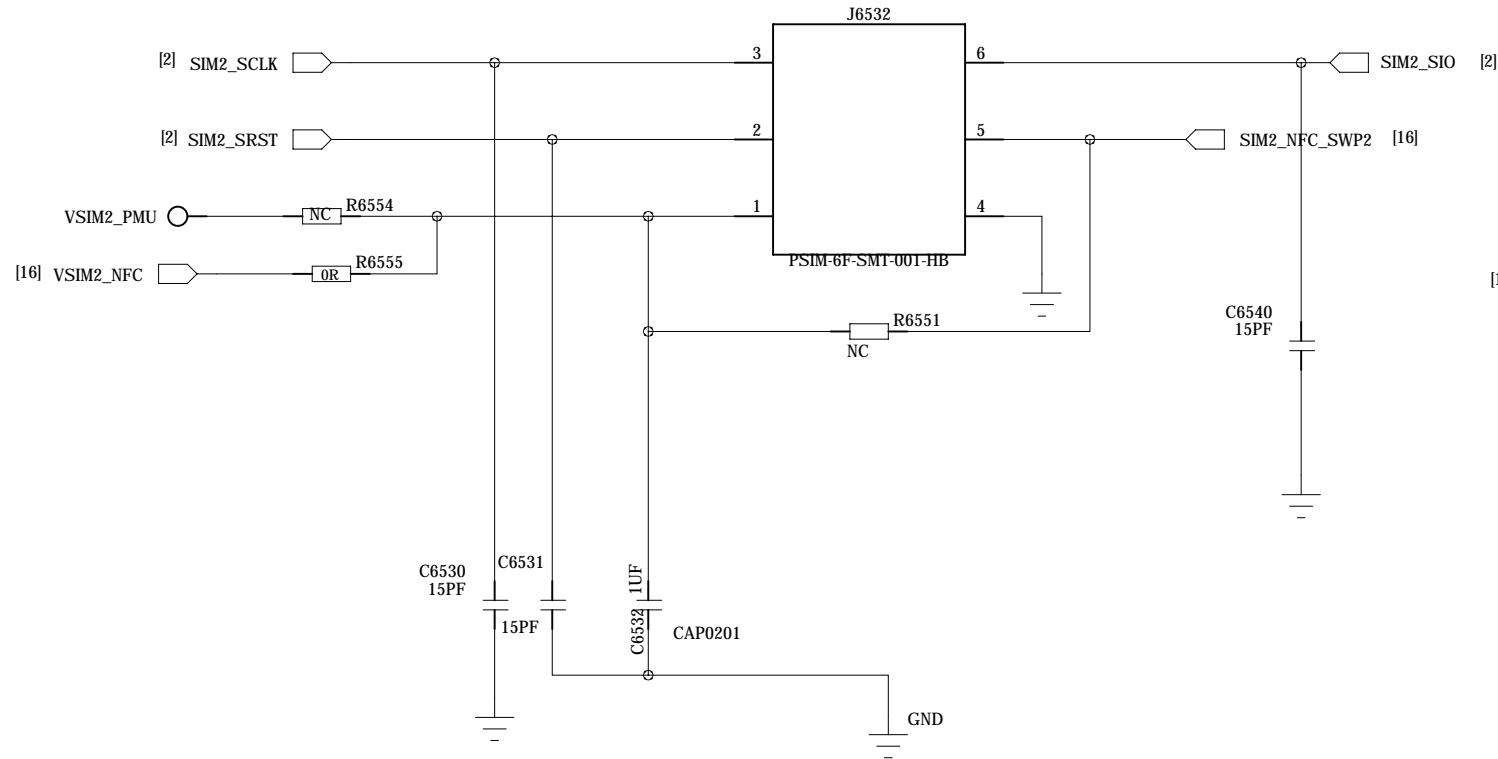




Power KEY



SIM2 Card



SIM1 Card

